Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 514-515

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High performance 50 nm $In_{0.65}Al_{0.35}As/In_{0.75}Ga_{0.25}As$ Metamorphic HEMTs with Si_3N_4 passivation on thin InGaAs/InP layer

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1. Introduction

Recently, there have been works about scaling down various component of HEMTs. A representative case is reduction of gate length. With lateral scaling like reduction of gate length, that is vertical scaling, gate to channel (G-C) spacing must be reduced to enhance ability of channel modulation. The various processes were tried to scale down G-C spacing like Pt annealing and etching barrier [1]. But, these processes have limit of process control and device characteristics. Another approach is barrier thinning in epitaxial structure. This approach also has problem with exposure of recessed region and plasma damage in passivation process. To solve this problem, we passivated recessed region and various problems in passivation process were solved with inserted thin InGaAs layer on InP etch stopper. With this epitaxial structure, We could get f_T=490GHz with fabricated 50nm MHEMTs .

2. Device fabrication and Hall measurement

The exposed surface of recessed region may lead to various problems such as degradation in electrical performance and physical damage, especially for epitaxial structure having thin barrier. Hence, the passivation is important to improve device performance, operation stability and long-term reliability. We adopted silicon nitride (Si_3N_4) as a passivation layer which is the most commonly used dielectric for InP-based transistor passivation. Similar to other semiconductor devices, the surface effects critically influence device performances of the HEMTs. The passivation with Si_3N_4 increases the surface Fermi level towards the conduction band-edge for InGaAs or InP. The Ns in channel of HEMTs is increased after Si_3N_4 passivation due to a decrease in surface potential. To make the good use of former advantage, the Si_3N_4 is deposited on exposed InP etch stopper. But, this passivation resulted in surface damage because NH3 plasma etches phosphorous preferentially [2]. To solve this problem, thin InGaAs layer is located on InP etch stopper to prevent surface problem. The epitaxial structure for device fabrication is shown in the Fig 1(a). Indium mole-fractions of 75% was applied to channel material and thin barrier (30Å) was adopted to reduce channel aspect ratio [3]. To lower sheet resistance, delta doping layers of $2x10^{13}$ cm^{-2} were applied in every 25 Å spacing inside upper InGaAs and InP cap layer. The gate structures of fabricated devices are shown in the Fig.1(b)-(d). The fabrication process of HEMTs is as follows. The process begins with mesa isolation using phosphoric etchant. For ohmic electrodes, Ni/Ge/Au were evaporated and followed by rapid thermal annealing at 320 ℃ for 30 s. Ohmic contact resistance and sheet resistance were 0.015 Ω mm and 45 Ω/□, respectively. The gate recess in the InGaAs and InP cap layer was formed by the citric acid solution and HCL solution, respectively. The Si_3N_4 (300 Å) passivation layer was deposited by remote plasma enhanced chemical vapor deposition (RPECVD). Before gate metal evaporation, InP etch stopper on the barrier was etched in Ar gas. Finally, the Ti/Pt/Au gate metal was evaporated and lifted off. The same structure for the device fabricated (fig. 1(b)-(d)) was characterized by Hall measurement before and after passivation. In fig. 3(a), The sheet carrier density (Ns) was improved most on device of fig. 1(d) by remote Pecvd, and next, by ICPCVD using low power and finally by ICPCVD using high power. The increase of Ns and mobility (Fig. 3(b)) shows increase of Ns in channel, in particular. In comparison of fig. 1(c) to fig. 1(d), there is a similar tendency in ICP conditions. However, the amount of increase in remote PECVD condition gets smaller than that of ICP conditions. This is because InP layer was degraded by phosphoric desorption on surface from NH_3 plasma. On the whole, for the case of passivation on the InP layer, the amount of increase in Ns is relatively small and the amount of difference in Ns between ICP conditions get even larger, compared to that on the passivation spacer. This results shows that plasma effect is severe as the layer which is passivated by Si_3N_4 gets closer to the channel and more sensitive among the different conditions in plasma. Among fig. 1(b)-(d), Fig. 1(d) shows superior characteristics concerned with passivation and can reduce plasma effect due to adding thin InGaAs passivation spacer.

3. Results

The DC and RF characteristics of fabricated 50nm MHEMT were plotted in Fig.4. The device characteristics of fig. 1(d) is as follows. The pinch-off voltage was -0.5 V. The maximum saturated current was about 750 mA/mm and the maximum transconductance $G_{m.max}$ was about 1.5 S/mm. The RF characteristics were determined by RT on-wafer measurement at frequencies up to 50 GHz using an HP8510C vector network analyzer and on-wafer probes. Fig. 4(b) shows the frequency dependence of the current gain H_{21}, and the maximum available gain (MAG/MSG) of the 50 nm gate MHEMT at Vds=0.7 V and Vgs=0 V. We obtained the unit current gain frequency f_T of 490 GHz by extrapolating H_{21} with a slope of -20 dB/decade. The maximum oscillation frequency f_{max} was estimated to be

about 270 GHz from MAG/MSG. $G_{m,max}$ and f_T of fig. 1(d) were improved by 6%, 11% compared with those of fig. 1(b) and 9%, 23% compared with those of fig. 1(c), respectively. The variations in the dc and rf characteristics are due to increase of Ns and decrease of trap by the surface states after deposition of the Si_3N_4 passivation film.

4. Conclusion

In this paper, thin InGaAs layer to prevent phosphorous deficiency maximizes passivation effect and fabricated 50nm MHEMTs showed the DC characteristics of V_{th} = -0.5V, $G_{m.max}$ = 1.5 S/mm and microwave characteristics of f_T=490GHz (Vds=0.8V, Vgs=0.2V) were extrapolated from the H_{21}.

Acknowledgements

This work was financially supported by the National program for Tera-Hz level Integrated Circuits of the Minister of Science and Technology as one of the 21st Century Frontier program

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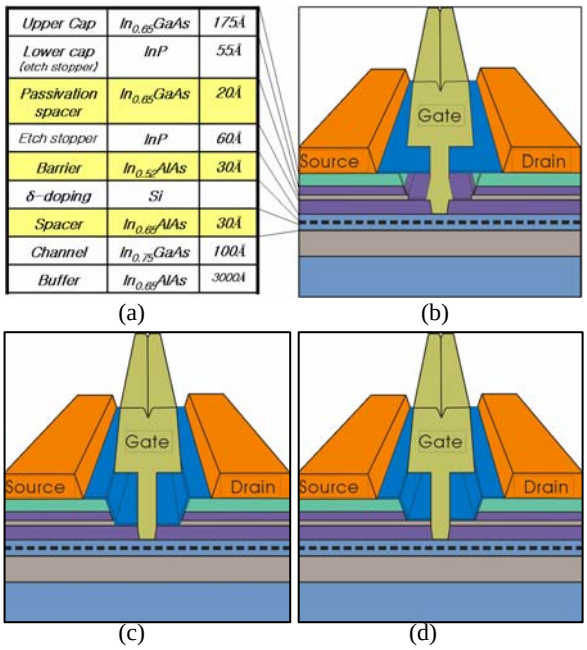

Fig. 1. Epitaxial structure and various recess structures (a) structure with thin InGaAs passivation spacer to enhance effect of passivation (b) conventional recess structure (c) passivation onto InP layer after recess structure (d) passivation onto passivation spacer after recess structure.

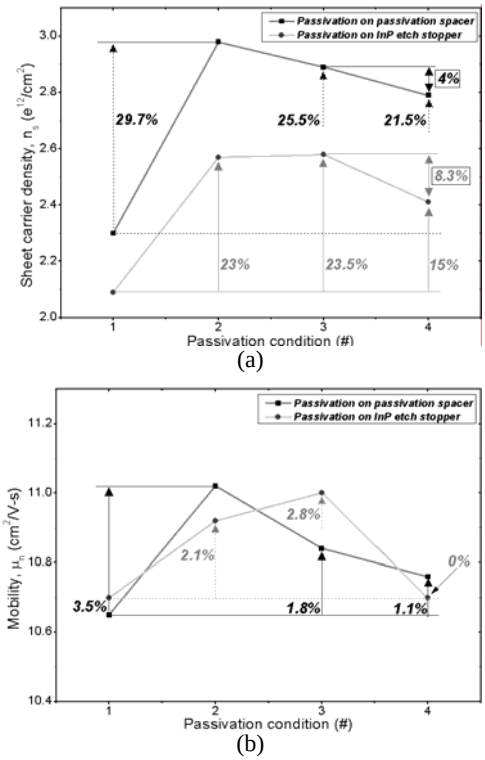

Fig. 3. hall measurement before and after passivation with various condition: (#1: before passivation, #2: Remote-PECVD, 50W, SiH_4/NH_3, #3: ICPCVD, 350W, SiH_4/N_2, #4: ICPCVD, 700W, SiH_4/N_2) (a) sheet carrier density (b) mobility

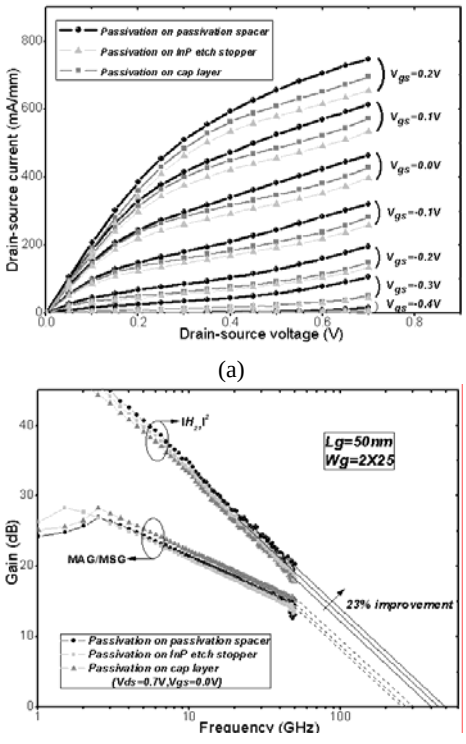

Fig. 5. DC and RF characteristics (two fingers, W_G=25um): $G_{m,max}$ of 1.5S/mm, $I_{d,max}$=750mA/mm, f_T of 490GHz (V_{gs}=0.0V, V_{ds}=0.7V) was extrapolated from H_{21} which was measured using HP8510C network analyzer.