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# High-speed and Low-Power SCFL-Type NRZ Delayed Flip-Flop Circuit Using RTD/HEMT Integration Technology

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## 1. Introduction

After MOnostable-to-BIstable transition Logic Element (MOBILE) was proposed [1], the monolithic integration of RTD and conventional transistors has attracted much attention for high-speed digital circuit application. And in order to enhance the compatibility to conventional SCFL-type circuits, MOBILE with SCFL-interface was proposed and its operation was confirmed up to 50 Gb/s by simulation [2]. However, MOBILE-based circuits are not compatible to conventional logic circuits because MOBILE-based logic circuits' outputs are return-to-zero (RZ) mode. To overcome this problem, CML-type NRZ-mode MOBILE-based D-F/F was proposed and the operation was confirmed up to 32 Gb/s using RTD/HBT integration technology [3]. However, the circuit complexity and power consumption increase compared to those of the original MOBILE circuit. To overcome this problem, we have previously proposed a new NRZ-mode D-F/F circuit using RTD/HEMT integration technology on an InP substrate [4]. Even though proposed circuits have the advantage of reduced device count and power consumption over the previously reported D-F/Fs, the output is single-ended. Thus the proposed circuits are not compatible to conventional SCFL circuits.

In this paper, we propose a new SCFL-type NRZ-mode D-F/F circuit with differential output with reduced circuit complexity and power consumption. The proposed circuit was fabricated using RTD/HEMT integration technology on an InP substrate. And the operation of the fabricated circuit was demonstrated up to 12.5 Gb/s.

## 2. Circuit configuration and operation principle

Figure 1 shows the circuit configuration of proposed NRZ D-F/F with differential output, which consists of two single-ended NRZ D-F/Fs and a SCFL-type current modulator. The operation principles of single-ended NRZ D-F/Fs were previously reported [4]. The key point of the proposed circuit is that the output state is determined at the rising edge of the clock and maintains its logic state when clock is high. When clock is low the output maintains its logic level by the self-latching characteristics of the RTD. For proper NRZ-mode operation, clock low level is designed properly to make the circuit bistable when clock is low.

The operation principle of the proposed circuit is as follows. When DATA is high, the current of the current source is flow through BMBTLE1 in Fig. 1. Thus the OUT1 latches to high and OUT2 latched to low at the rising edge of the clock. When DATA is low, the current of the current source is flows through BMBTLE2 in Fig. 1. Thus OUT1 latches low and OUT2 latches to high in this case. Conseq-,

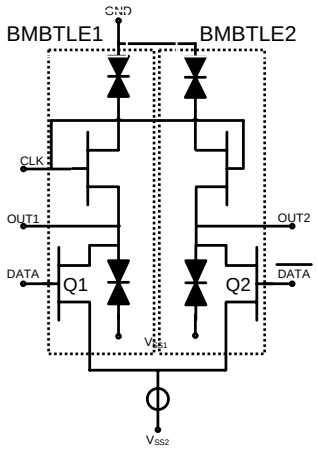


Fig. 1 Circuit configuration of proposed NRZ D-F/F

uently the proposed circuit functions as SCFL-type D-F/F which generates differential NRZ-mode outputs according to input signals.

## 3. Device structure and fabrication

We integrated AlAs/InGaAs/InAs RTD and InAlAs/InGaAs HEMT monolithically on an InP substrate. The epitaxial layers were grown by MBE and the devices were fabricated using optical lithography, e-beam lithography and lift-off process. Figure 2 shows the cross-sectional view of the fabricated ICs.

The peak current density of the fabricated RTDs was 112 kA/cm$^2$ with a good peak-to-valley current ratio of 12. The peak voltage of the fabricated RTD was 0.3 V. Fabricated 0.1 um HEMT showed the maximum transconductance of 1.2 S/mm with the threshold voltage of -0.55 V. The maximum cutoff frequency was about 220 GHz.

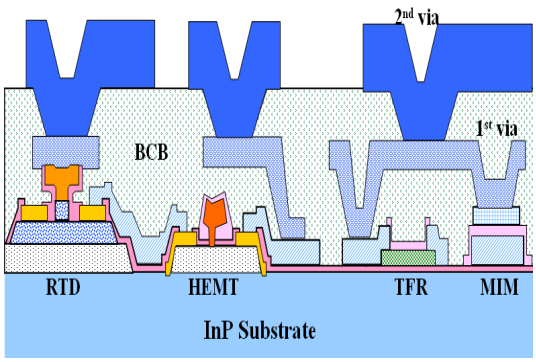


Fig. 2 Cross-sectional view of the fabricated ICs

## 4. Measurement result

Figure 3 shows the micro-photograph of the fabricated ICs. To minimize measurement system effect, we included input/clock/output buffers in the test circuit. We used simple 50 ohm resistor for input and clock buffers. And DCFL inverters with 100 ohm load resistor for output buffers.

In order to demonstrate the operation of the fabricated D-F/F circuit at 12.5 Gb/s, a pulse pattern generator (Anritsu-MP1763B) was used to obtain the data stream and clock. The output of the fabricated circuit was fed into a digital communication analyzer (Agilent 83484A). Figure 4 shows the output bit stream at 12.5 Gb/s with an input bit pattern of (11011100). The upper trace shows the inverted output bit stream and the lower trace shows the non-inverted output bit stream. The bit stream of the non-inverted output port is complement of the input bit stream because the output buffer acts as inverter. And the bit stream measured at the inverted output port is same as input bit stream due to output buffer. The output amplitude was about 125 mV for both non-inverted and inverted outputs.

The measured eye-diagram for 12.5 Gb/s $2^{31}$-1 PRBS (pseudo-random bit stream) input signal is shown in Fig. 5. Clear eye-diagrams with about 125 mV eye-opening were obtained for both non-inverted and inverted output. These results confirm the proper operation of the proposed SCFL-type NRZ D-F/F up to 12.5 Gb/s.

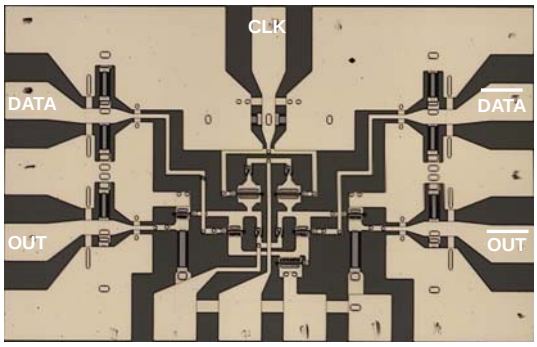


Fig. 3 Micro-photograph of the fabricated ICs

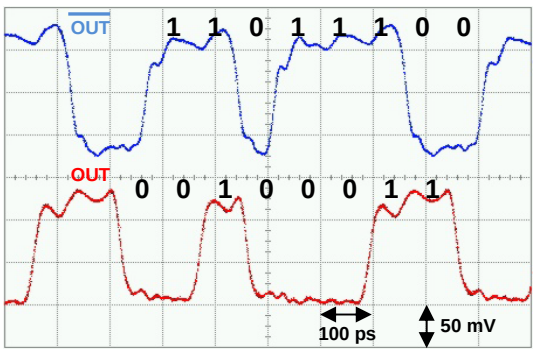


Fig. 4 Measured output bit-stream at 12.5 Gb/s

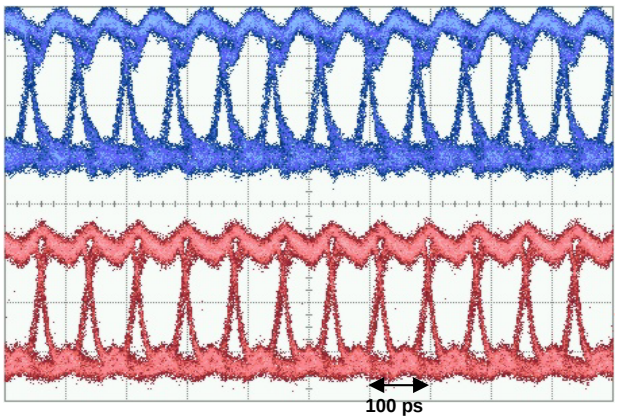


Fig. 5 Measured output eye-diagram at 12.5 Gb/s

## 5. Conclusion

A new SCFL-type NRZ D-F/F circuit with drastically reduced circuit complexity is proposed and fabricated using RTD/HEMT integration technology on an InP substrate. The proposed circuit uses only 9 devices (4 RTDs and 5 HEMTs) with one logic stage, by utilizing switching and self latching properties of RTDs, which is the minimum device count to implement NRZ D-F/F with differential outputs up to now. The operation of the fabricated circuit was confirmed up to 12.5 Gb/s. And the power consumption of the fabricated D-F/F core circuit is about 11 mW at 12.5 Gb/s. The proposed circuit enhances the compatibility of the RTD/HEMT NDR digital ICs with conventional SCFL-type circuits. This result indicates the great potential of the proposed circuit for high-speed and low-power digital IC applications.


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