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Novel Vacuum Encapsulation Applied for Improving Short-Channel Immunity on Poly-Si Thin Film Transistors

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Abstract

A novel T-shaped-gated (T-Gate) polycrystalline silicon thin-film transistor (poly-Si TFT) with in-situ vacuum gaps has been proposed and fabricated only with a simple process. The T-Gate structure is formed only by a selective undercut-etching technology of the Mo/Al bilayers. Then, vacuum gaps are in-situ embedded in this T-Gate structure subsequent to capping the SiH₄-based passivation oxide under the vacuum process chamber. The proposed T-Gate poly-Si TFT has demonstrated to suppress the short-channel effect and to improve the breakdown characteristics. It is attributed to the undoped offset region and vacuum gap to reduce the maximum electric field at drain junction.

1. Introduction

Poly-Si thin film transistors (TFTs) have been widely used as switching elements in active matrix displays. For the further development, high versatile circuits and systems need to be fully integrated on the display panel substrate, which is the concept of systemon-panel (SOP). As performance and complexity requirements increase, there is a need to scale down device geometries to achieve higher speeds and packing densities. Unfortunately, it has been shown that conventional short-channel poly-Si TFTs suffer from undesirable effects the several in electrical characteristics, including the threshold-voltage (Vth) roll-off effect, and poor breakdown characteristics. Those all are increased with the higher drain electric field near the drain junction. These undesirable effects prohibit the use of LTPS TFTs in many highperformance circuit applications.

In this work, novel vacuum (the lowest permittivity of k=1 in nature),⁵ which is in-situ embedded in a T-gate structure, is applied to suppress the short-channel effect. And, the T-shaped-gated (T-Gate) poly-Si thin-film transistor with self-aligned sub-gates is fabricated only with a simple selective-etching process and without any additional photo-lithography step.⁶

2. Device Fabrication

The process sequence of the proposed T-Gate poly-Si TFT with vacuum gaps is illustrated in Fig.1. At first, the 1000Å-thick a-Si thin film was deposited on oxidized silicon wafer by decomposition of SiH₄ with LPCVD at 550°C. Then, the a-Si thin film was transferred into poly-Si by a solid phase crystallization at 600°C for 24 hours. After defining the active layer, a 1000Å-thick TEOS gate oxide was deposited. Then, a 600 Å-thick Al, and a

2000Å-thick Mo films were deposited by sputter system sequentially. The stacked Mo/Al films were simultaneously etched by reactive ion etching (RIE) to pattern the gate electrode [Fig. 1(a)]. A self-aligned phosphorous implantation with dose of 5×10^{15} cm⁻² was carried out to form source and drain regions, and then excimer laser irradiation was employed to activate the dopants. H₃PO₄ solution is then used to selectively etch the Al layer without harming Mo layer to form a Tshaped structure. H₃PO₄-solution etching process at 35°C is controlled carefully using time-mode, which was confirmed by SEM-monitoring the relation between the Al side-etching length and the etching time, as shown in Fig. 1(c). In this work, using the H₃PO₄-solution immersion for 210 seconds, a symmetrical T-shaped gate electrode can be simply conducted by the selective etching for the Al film of 0.5 µm in length under the Mo layer from the two-side of this patterned gate.⁶ For the purpose of comparison, the conventional poly-Si TFTs without side-etching structure were also fabricated.



Fig. 1. (a) the formation of the T-Gate structure, and (b) the in-situ vacuum gaps creation via capping the SiH₄-based dielectric in PECVD system, (c) the side-etching length dependence on the etching time, and (d) the SEM photograph of the cross-section of the T-Gate structure with symmetrical in-situ vacuum gaps.

Then, all TFTs were subjected to the NH_3 plasma treatment to reducing the trap-states of the poly-Si film. Sequentially, a 5000Å-thick SiH₄/N₂O oxide and a 2000

Å-thick SiH₄/NH₃ nitride were deposited under a 400 m-torr vacuum chamber in PECVD system as the passivation and seal layers, respectively. It should be noted that the SiH₄ free radicals are very active and chemisorbed on the substrates easily,⁸ making SiH₄-based passivation oxide difficult to be filled under the side-edge of Mo layer, and thus resulting in the in-situ formation of the vacuum gaps during this process [Figs. 1(b) and 1(d)]. Contact opening formation and metallization were carried out. By the way, the proposed TFT has the same photo-lithography steps as the conventional one.

3. Results and Discussion

In order to study the short channel effect of T-Gate TFTs and conventional TFTs, the transfer characteristics with different channel length are measured, as shown in Figs. 2(a) 2(b). The threshold voltage of T-Gate TFTs and and conventional TFTs are also extracted and compared, as shown in Fig. 3. It is noticed that the threshold voltage of conventional TFTs decrease from 5.7 V to 1.1 V when channel length is reduced from 10 µm to 1.5 µm. For T-Gate TFTs, the threshold voltage of 6.0 V and 4.9 V are obtained in device with 10 μ m and 1.5µm channel length, respectively. The threshold voltage shift on conventional TFTs is 82%, but the shift on T-Gate TFTs is only 19%. This is well-known that the small dimension poly-Si TFTs suffer a severe drain avalanche multiplication due to the high drain electric field.¹⁻³ Consequently, T-Gate TFTs reduce drain electric field effectively and therefore suppress the threshold voltage roll-off for the short channel effect.



Fig. 2. Transfer characteristics of (a) T-Gate TFTs and (b) conventional TFTs for various channel lengths, respectively.



Fig 3. Threshold voltages as a function of channel length for conventional TFTs and T-Gate TFTs.

Besides, Figs. 4(a) and 4(b) show the measured drain breakdown characteristics of T-Gate TFTs and conventional TFTs with different channel lengths. The drain breakdown voltage of T-Gate TFTs and conventional TFTs are also extracted and compared, as shown in Fig. 5. The breakdown voltage is defined as the drain voltage when the drain current equaled to 2 nA with $V_{GS} = 0V$, for both conventional and T-Gate TFTs. It can be found when the channel length reduces from 10 μ m to 1.5 μ m, the drain breakdown voltage for conventional TFTs decreases from 13.3 V to 7.1 V (reduce 47%), while only from 17.8 V to 11.7 V (reduce 35%) in breakdown voltage is observed for T-Gate TFTs. The

improvement of the drain breakdown voltage can be obtained by T-Gate TFTs. It is attributed to the offset region of T-Gate TFT brings about smaller lateral electric field than conventional TFTs.⁴ The improved breakdown characteristics imply that the T-Gate TFTs are suitable for channel length scaled down for high performance digital circuit applications.



Fig. 4 (a) Drain breakdown characteristics of (a) T-Gate TFTs and (b) conventional TFTs at V_{GS} = 0V for various channel lengths, respectively.



Fig. 5 The breakdown voltage as a function of channel length for conventional TFTs and T-Gate TFTs.

4. Conclusions

In this work, a novel T-Gate poly-Si TFT with in-situ vacuum gaps has been proposed and fabricated with a simple procedure. The T-Gate structure is fabricated by a selective etching technology of the Mo/Al bi-layers. Then, vacuum gaps are in-situ embedded in this T-Gate structure subsequent to the capping of the SiH₄-based passivation oxide under a vacuum process chamber. The proposed T-Gate TFTs have excellent electrical performance. It is well known that drain breakdown phenomenon and Vth roll-off of short channel effect are attributed to the severe impact ionization caused by large drain electric field. From the experimental results, T-Gate TFTs have better immunity to threshold voltage roll-off and larger breakdown voltage. Therefore, such a T-Gate poly-Si TFT is very suitable for the applications and manufacturing in active-matrix flat panel electronics.

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