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A Quasi-planar Thin Film Field Emission Diode

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***Abstract* --** A novel quasi-planar thin-film field emitter is fabricated utilizing thin-film deposition and wet etching processes. The spacing between the emitter and collector could be well controlled via the thickness of Cr layers, which creates sub-micron gap. A forming process causes an increased surface roughness of emitters and results in a higher field enhancement factor, which shows better field emission characteristics. The turn-on voltage (at which the current level is 100 nA) of the device with the Cr thickness of 300 nm is as low as 12 V.

1. Introduction

Recently, there has been a great amount of interest in vacuum microelectronic (VME) devices due to their high tolerance to high temperature and high radiation environment than solid state devices. Two types of VME devices have been proposed: vertical and lateral (planar) type. Vertical type field emission devices have the difficult in incorporation with the collector electrode, and therefore require a series of complicated processing steps to form a cantilevered electrode.[1)] In the contrary, lateral (planar) field emission devices have attracted considerable attention in vacuum microelectronics due to ease of fabrication, design versatility of electrode geometry, and precise control of spacing between electrodes. A small spacing between electrodes is required for the reduction in the operation voltage of lateral field emission devices, thereby a lower power consumption. There have been several methods reported to create the small gaps. A subtenth-micron emitter to anode spacing could be fabricated by using high resolution electron beam lithography (EBL) in combination with a lift-off process.[2)] Gotoh *et al.* employed a focus ion beam (FIB) technique for the fabrication of lateral-type thin-film edge field emitters.[3,4)] Lee et al. proposed a novel sub-micron gap fabrication technology using chemical-mechanical polishing (CMP) to fabricate lateral field emission devices.[5)] However, a low throughput is generally limited for the fabrication processes via EBL and FIB techniques. A high-temperature oxidation process is necessary for the CMP technique, and cause a high thermal budget.

The objective of this work is to fabricate a field emission diode which could operate at a low voltage and have a well-controlled sub-micron spacing between the emitter and collector without using complicated manufacturing processes and instruments.

2. Experiment

Figure 1 shows the schematic diagram of the fabrication procedure of a quasi-planar field emission diode. A first metallic thin film of chromium (Cr, 300 nm) and an insulated silicon oxide layer (500 nm) were sequentially deposited on a N-type silicon substrate by E-beam evaporation and plasma-enhanced chemical vapor deposition (PECVD), respectively (Fig. 1(a)). The thickness of Cr thin film was used to define and control the spacing or the gap distance between the emitters and collectors. After photolithography, the silicon oxide layer and the first Cr thin film were isotropically wet-etched so as to form an undercut (Fig. 1(b)). The lateral etching distance of the first Cr layer should be larger than that of silicon oxide, thus forming a micro-cavity of Cr layer under the overhang of silicon oxide. Then, a second Cr layer with the thickness of 100 nm was deposited for the formation of emitter and collector (Fig. 1(c)). Finally, a forming process was employed for treatment of the second Cr layer (Fig. 1(d)). During the forming process, samples loaded into a quartz tube were heated to a temperature of 550℃ and kept for 30 min in a gas mixture of H_2 (100 sccm) and C_2H_4 (50 sccm).

3. Result and discussion

The cross-sectional and top-view SEM images of a quasi-planar filed emission diode are shown in Fig. 2. In order to precisely control the field emission area, the measured device has an emission edge of 200 μm in length via photolithography pattering (Fig. 2(b)). Figure 3 shows a schematic diagram of the measurement system and a quasi-planar field emission diode. Electrons are emitted from the emitter to the collector by applying a driving voltage (V_d) in a high vacuum chamber with a pressure below 5×10^{-6} torr. Field emission measurement was carried out with a diode-type configuration, and the emission current versus driving voltage is shown in Fig. 4. The device treated with forming process shows better field emission characteristics than that without forming process. As mentioned above, the surface morphologies treated by forming process presented a larger roughness than those un-treated. An emission surface having rougher morphologies possesses a higher field enhancement factor and more emission sites than flat one, thereby showing a better property. The turn-on voltage (V_{to}) at the emission current of 100 nA for the device with forming process is estimated to be 12 V, and an emission current of 8 μA could be achieve as the driving voltage applied to 20 V.

4. Conclusion

A novel structure of quasi-planar field emission diode formed of Cr thin film is fabricated by thin-film deposition and wet etching processes. Devices treated with a forming process at the temperature of 550℃ have a surface morphology rougher than those un-treated due to the formation of carbides, which could significantly improve the field emission property.

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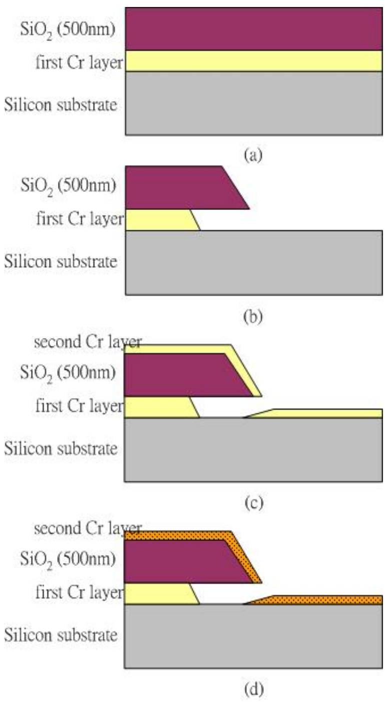

Fig. 1. A schematic diagram of the fabrication procedure of a quasi-planar field emission diode.

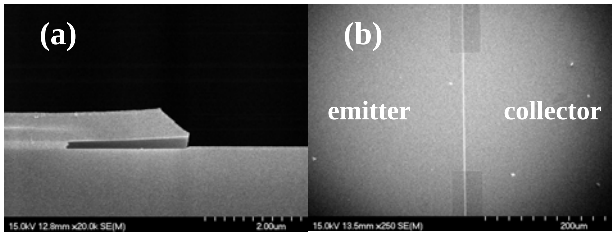

Fig. 2. (a) The cross-sectional and (b) top-view SEM images of a quasi-planar filed emission diode.

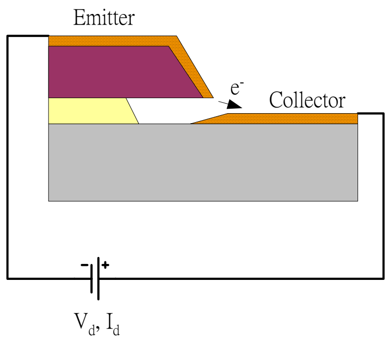

Fig. 3. A schematic diagram of the measurement system and a quasi-planar field emission diode.

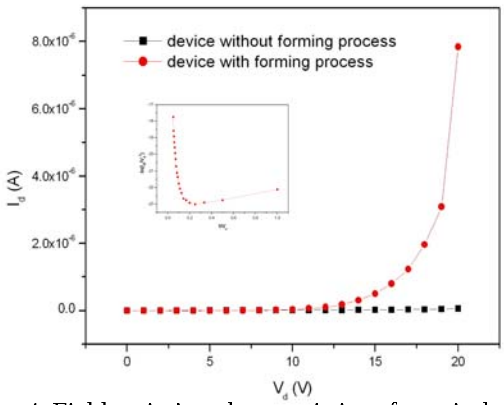

Fig. 4. Field emission characteristics of quasi-planar field emission devices with and without forming process.