

Current and Speed Enhancements at 90nm Node through Package Strain

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1. Introduction

Strained-Si technology can enhance the carrier mobility of MOSFET devices without scaling down the devices. The process strain obtained by a silicon nitride cap, silicide, and SiGe source/drain is now used in the production of 90nm node CPU products [1]. However, the advantages of the process strain diminish in large devices such as at the 180nm or 250nm nodes. The substrate strain, which is induced by SiGe buffer layers underneath the silicon circuitry, causes the thermal budget to suffer, induces threading defects, and has a high cost. We have demonstrated that external mechanical stress can provide package strain on long channel MOSFET devices and enhance device performance [2]. To integrate package strain into the circuit application, the relative channel layout of NFET and PFET has to be taken into consideration.

2. Package strain methodology

A 65-stage ring oscillator with Cu interconnect is also fabricated using 90nm nominal and process-strained process [3] with $f_T \sim 100\text{GHz}$. The process-strained process includes a high-tensile ILD nitride-cap layer. The ratio of width for the PFET to the NFET in each stage is 1.5 for 90nm process to compensate for the mobility mismatch in each inverter stage. Fig. 1 shows the schematic diagram of the setup to provide package strain. The glue between the chips and package substrate is selected to allow stress to propagate into the chips from the package substrate.

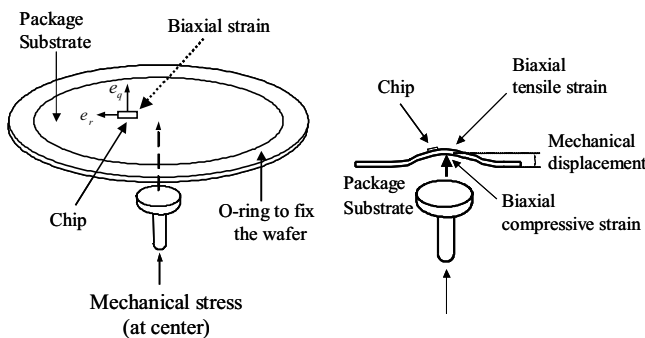


Fig. 1 Schematic diagram of the externally applied biaxial-mechanical stress. The glue between devices and package substrates is selected to allow the stress to propagate into the chips from the package substrate.

Fig. 2 shows that the strain at different mechanical displacements can also be observed from Raman spectra of package Si substrate with known properties.

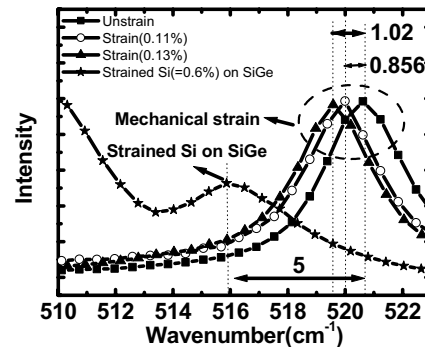


Fig. 2. Raman spectra of the mechanically strained Si. The position of Si-Si peaks of strained Si indicate 0.11% and 0.13% biaxial tensile strain. Strained Si on $\text{Si}_{0.8}\text{Ge}_{0.2}$ buffer is also shown for reference.

Moreover, the strain gauge [4] and finite element simulation by ANSYS are also used to measure the strain on the package substrate. Fig. 3 reveals that there is good agreement between simulation and measurement for biaxial tensile strain generated by central displacement.

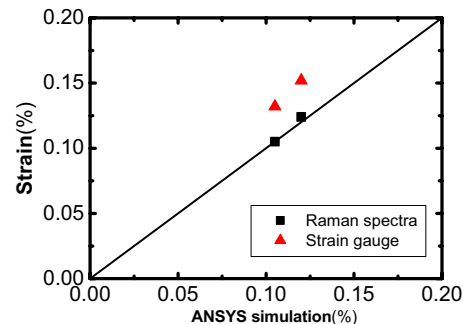


Fig. 3 Strain measured by Raman spectra, strain gauge and simulated by ANSYS. There is a good agreement between simulation and measurement.

Other strain conditions in this study are analyzed by ANSYS simulation. Fig. 4 shows the electroluminescence (EL) spectra at 120K from the unstrained/strained MOS LED samples. The bandgap of strained Si is reduced by 15 meV under 0.13% biaxial tensile strain. The higher EL intensity of strained Si LED indicates that no defect is generated during the strain, and the valence band edge shifts upwards.

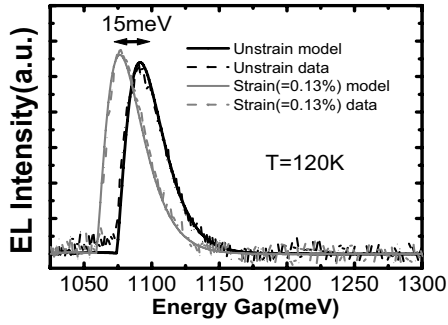


Fig. 4. The measured electroluminescence spectra of relaxed/strained MOS LED with fitting curves of the electron-hole plasma recombination model.

3. 90nm device performance

The output characteristics of 90nm node NFET is shown in Fig. 5 and the gate length is 70nm. There are 4.9% and 3.7% current enhancements under 0.096% biaxial tensile strain for nominal and process-strained NFET devices, respectively.

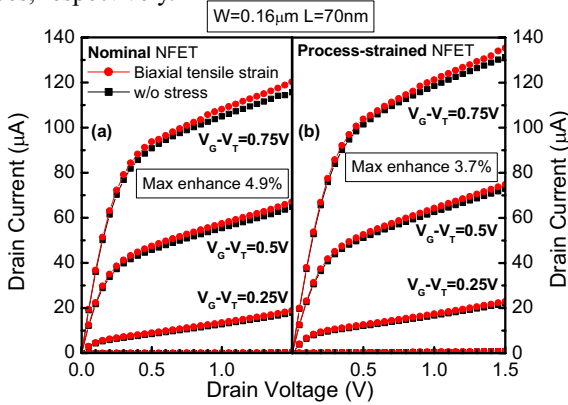


Fig. 5 The change in drain currents for (a) nominal and (b) process-strained NFET ($W \times L = 0.16 \times 0.07 \mu\text{m}^2$) with the biaxial tensile strain ($\sim 0.096\%$). The process-strained devices have a modified high-tensile (1.5GPa) ILD nitride layer.

Fig. 6 displays that the current enhancement under biaxial tensile strain is also nearly independent of the NMOS device widths. The process-strained NFET devices, which have a modified high-tensile (1.5 GPa) ILD nitride layer, show a smaller current enhancement than the nominal ones due to the pre-strained condition [5]. The 90nm node PFET devices are also measured under biaxial tensile strain. However, there is no significant current enhancement.

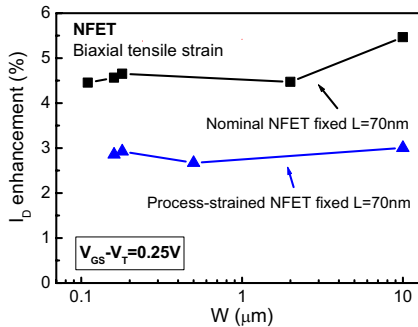


Fig. 6. The drain current change in saturation region of 90nm node NFET devices with various gate widths under biaxial tensile strain ($\sim 0.096\%$). The enhancement is nearly independent of gate width.

The delay time of the ring oscillator is 16.9 ps. The speed enhancement of the ring oscillator under biaxial tensile strain is shown in Fig. 7. There are 2.3% and 1.5% speed enhancements under 0.096% biaxial tensile strain for nominal and process-strained ring oscillators, respectively. The speed enhancement should be larger if the perpendicular layout is used since both NFET and PET can be improved simultaneously. Fig. 7 also reveals the speed enhancement increases as the mechanical strain increases.

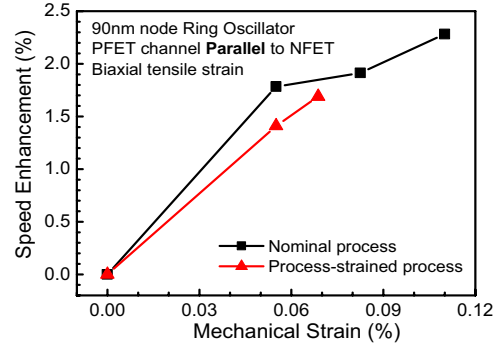


Fig. 7 The measured speed enhancement of 90nm node ring oscillator with parallel layout under various package strains.

Finally, Fig. 8 shows that the leakage current from drain to body will slightly increase under biaxial tensile strain. This is also due to the reduction of Si bandgap, as shown in Fig. 4. However, compared to the drain current, this leakage current is very small and can be neglected.

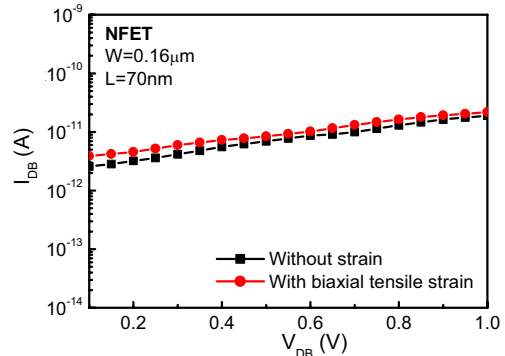


Fig. 8. The drain-to-body leakage current of 90nm node NFET device. The device under biaxial tensile strain ($\sim 0.096\%$) has slightly higher leakage current.

4. Conclusion

The interaction between circuit design and package strain is comprehensively studied in this work. It is demonstrated for the first time that the speed of 90nm node circuitry can be enhanced by external package/mechanical strain, and its speed enhancements is 2.3%. The package strain is inexpensive and gives reasonable speed enhancement, suggesting a new technique for providing strain for 90nm technology node and beyond.

References

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