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A Physics-based Compact Model for I-MOS Transistors

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1. Introduction

Since the impact-ionization MOS (I-MOS) transistor was first proposed [1], it has attracted much attention as a promising technology for achieving abrupt subthreshold swings much lower than kT/q [1-7]. However, all studies to-date focus on experiments or device modeling using TCAD. Few equations were formulated to describe its first-order characteristics in DC, and, more importantly, in transient and AC operations.

In this paper, we report the first physics-based compact model for an SOI-based I-MOS transistor that works in both DC and transient regimes. The model is implemented with macros in HSPICE, and is suitable for studying the performance I-MOS devices in circuits beyond a few transistors.

2. Construction of the Compact model

The macro model for I-MOS (Fig.1c) is constructed by considering both the electrostatic and the transport equations.

Electrostatics

The IMOS transistor is partitioned into two segments [Fig. 1(a)], one under the gate ($0 < x < L$), and the other without gate control ($-L_I < x < 0$). Quasi-2D analysis of Poisson equation is applied to active region [8], with the assumption of constant lateral E-field in the breakdown region ($-L_I < x < L$), and a thin layer of carriers of uniform density ρ under the gate. The surface potential at the boundary of the gate [$x = 0$ in Fig.1(a), and node 102 in Fig. 2] is thus derived to be

$$\phi_{x=0} \approx \frac{L_I}{L_I+\lambda}\phi_s + \frac{L_I}{L_I+\lambda}\left(1-2e^{-\frac{L}{\lambda}}\right)\left(\phi_g - \frac{\eta}{\varepsilon_{si}}\rho\lambda^2\right) + \frac{L_I}{L_I+\lambda}2e^{-\frac{L}{\lambda}}\cdot\phi_d, \tag{1}$$

where λ is the characteristic scaling length, φ_s and φ_d are the potentials at source and drain, respectively, and η is a fitting parameter. To account for the inversion charge near the drain end of the channel before breakdown occurs, an empirical term $-\gamma H(\varphi_s - \varphi_d)^2$ is appended to eq.(1), involving the step function H, and a fitting parameter γ.

Continuity equation

Unlike a normal MOSFET, where we almost always assume quasi-static carrier concentration in the channel, I-MOS operates in highly non-equilibrium situation. Therefore, it is essential to start from the carrier continuity equations in order to correctly model the device in transient. We start from the electron continuity equation, $dn/dt = 1/q(dJ_n/dx) + G - R$, where we assume velocity saturation ($J_n = qnv_{sat}$) throughout the active region. With finite volume descretization around a volume i of length Δx, the continuity equation reads,

$$\frac{d(\Delta x\cdot\bar{n})}{dt} = \frac{\Delta x}{2qv_{sat}}\frac{d(J_{n,L}+J_{n,R})}{dt} = \frac{1}{q}(J_{n,R}-J_{n,L}) + \Delta x\cdot(G-R), \tag{2}$$

where $J_{n,L}$ and $J_{n,R}$ are the electron current at the left and right end of the volume, respectively. One can immediately recognize Kirchhoff-Current-Law from eq. (2):

$$J_{n,R} - J_{n,L} + J_{G\text{-}R} - J_{dn} = 0, \tag{3}$$

$$J_{dn} = \frac{\Delta x}{2v_{sat}}\frac{d(J_{n,L}+J_{n,R})}{dt}, \tag{4}$$

as illustrated in Fig. 1(b).

The electron and hole continuity equations in the two segments of the I-MOS are thus constructed as shown in Fig. 2, by applying eq. (3) to each segment. The time derivatives of the currents are measured by the voltage across inductors (e.g. L_{n1}), and J_{dn} is then calculated with the dependent current sources (e.g. G_{dn1}). Some equations used in the macro circuit model are listed in Fig. 2. Note that the generation rate due to impact ionization (G_{ii}) depends on both voltage and the instantaneous currents, which is essential for modeling the transient behavior of I-MOS device/circuits.

3. Verification of the Compact Model

The proposed compact model for I-MOS is tested against TCAD simulation results. Medici is used to simulate the I-MOS device in both steady-state and transient mode, using the drift-diffusion equations, and electric-field based Chynoweth model for impact ionization rates.

In Fig. 3, the DC transfer characteristics obtained from TCAD and the compact model are compared. The correct V_d dependence of V_{th} (breakdown) voltage is shown. Above V_{th}, drain current increases with a transconductance G_m almost independent of drain voltage, which is a direct result of velocity saturation in the channel. In Fig. 4, the transient behavior of I-MOS in a resistor-loaded inverter is compared. It is learnt from TCAD that the transient drain current deviate significantly from that in steady-state under the same gate and drain biases, in drastic contrast to MOSFETs. Note that the proposed model is able to capture the following characteristics observed in TCAD:

1. The turn-on of drain current in transient operation lags behind that expected in DC operation, by ~40 ps.
2. The output voltage and drain current oscillates (and damps) around the steady-states value.

It should be pointed out that the above transient behaviors are direct results of the J_{dn} term in eq. (3), which is the physical basis of the proposed model. The delay of the resistor-loaded inverter obtained for a few combinations of input and load impedances is summarized in Table I. Excellent agreement between TCAD and compact model is demonstrated.

4. Conclusion

A physics-based compact model is proposed for I-MOS transistors. First-order device operation is very well described by the model in both DC and transient. Since the model is constructed around the basic semiconductor equations, future improvements on the model can be carried out in a systematic manner, which would further our understanding on the device physics of I-MOS to a great extent, and will allow performance evaluation of larger circuits.

References

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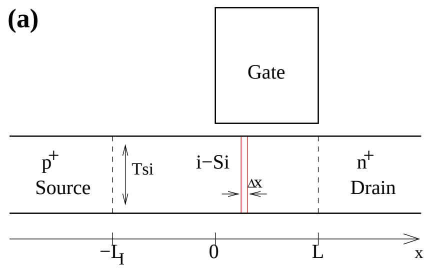

$$\frac{d^2\phi}{dx^2}-\frac{1}{\lambda^2}\phi+\left(\frac{1}{\lambda^2}\phi_g-\frac{\eta}{\varepsilon_{si}}\rho\right)=0$$

$$\lambda=\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{T_{si}T_{ox}}{\eta}}$$

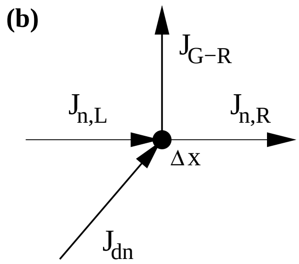

Fig. 1. Construction of the compact model for the I-MOS transistor. (a) The first step involves the quasi-2D solution of the Poisson equation in the SOI I-MOS device structure. (b) The second step involves solving the continuity equation for the carriers (only the electron version is shown) in a segment of the length, Δx, being discretized and modeled by Kirchoff's Current Law (KCL).

$$V_{102}=\frac{L_I}{L_I+\lambda}V_{104}+\frac{L_I}{L_I+\lambda}\left(1-2e^{-\frac{L}{\lambda}}\right)\left(V_2-\frac{I(Ln1)}{GM}\right)+\frac{L_I}{L_I+\lambda}2e^{-\frac{L}{\lambda}}\cdot V_{100}-\gamma\,\mathrm{H}(V_2-V_{100})^2$$

$$\mathrm{Q}_{\mathrm{Cgd}}=C_{gd1}(V_2-V_{102})+\mathrm{C}_{\mathrm{gd2}}(V_2-V_{100})$$

$$\mathrm{G}_{\mathrm{ii1}}=\alpha_{II}\exp\left(-V_{crit}/|V_{100}-V_{102}|\right)\left(|\mathrm{I}(\mathrm{L}_{\mathrm{n2}})|+|\mathrm{I}(\mathrm{L}_{\mathrm{p1}})|\right)+G_0$$

$$\mathrm{G}_{\mathrm{ii2}}=\alpha_{II}\exp\left(-V_{crit}/|V_{102}-V_{104}|\right)\left(|\mathrm{I}(\mathrm{L}_{\mathrm{p1}})|+|\mathrm{I}(\mathrm{L}_{\mathrm{n2}})|\right)+G_0$$

$$G_{dn1}=\frac{1}{2v_{sat}}\left(\frac{V_{201}-V_{100}}{L_{n1}}+\frac{V_{202}-V_{201}}{L_{n2}}\right)$$

$$\cdots$$

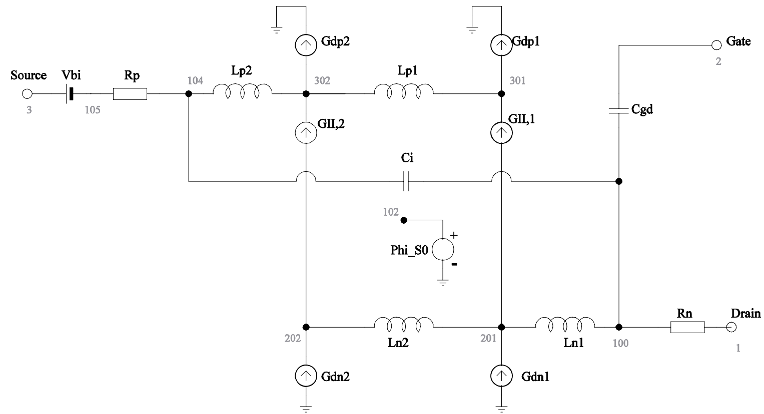

Fig. 2. Final step in compact model construction: Assembling the electrostatic and transport components. Inductors are only used for the purpose of measuring time-derivatives of currents, values of which are given by $L=L_0\Delta x$, with some arbitrary L_0. Expressions for the important dependent sources are listed.

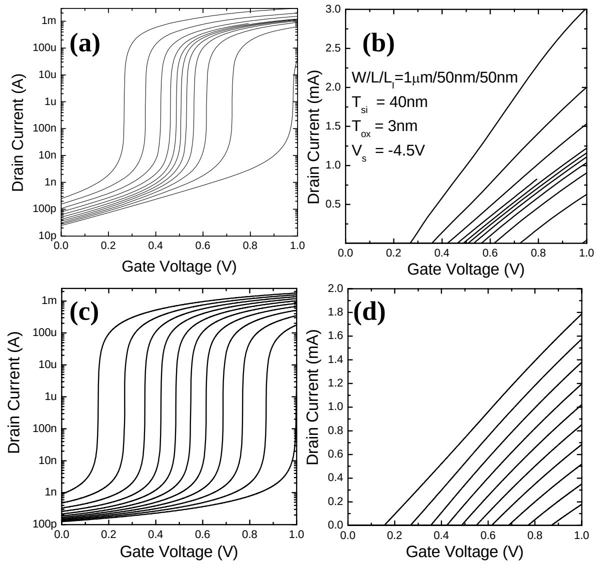

Fig. 3. DC transfer characteristics obtained from TCAD simulation [(a) and (b)], as compared with the result obtained from the compact model [(c) and (d)]. The dimension of the transistor is indicated.

Table I. Comparison of the delay obtained from TCAD and the compact model, using the above resistor-loaded inverter, showing excellent agreement.

R_{in} (kΩ)	R_{load} (kΩ)	C_{load} (fF)	$\tau_{50,TCAD}$ (ps)	$\tau_{50,model}$ (ps)
10	10	10	43	41
10	10	100	80	82
10	100	10	42	40
10	100	100	79	81

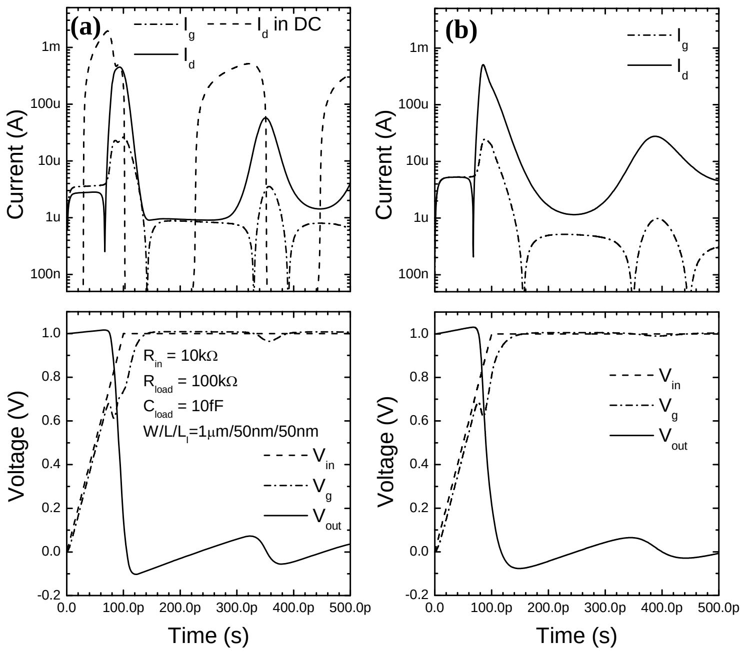

Fig. 4. Transient characteristics from (a) TCAD and (b) compact model of the (c) resistor-load inverter circuit (right), and using the same transistors as in Fig. 2. The ramp-up time for input voltage is 100 ps. The DC drain current is simulated in TCAD at the same gate and drain bias at each moment, and is plotted as dashed line in (a). Note the transient drain current does not follow that in DC, and exhibits a delay of about 40 ps.