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High-k Gated Germanium Metal-Oxide-Semiconductor Capacitors with GeO_2 Surface Passivation and Fluorine Incorporation

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1. Introduction

Germanium (Ge) substrate is increasingly being studied for MOSFET applications because of its high intrinsic carrier mobilities [1]. As the devices further scales down, high-k materials are considered as alternative gate dielectric layers. To build high quality high-k gate stack on Ge substrate, one of the critical challenges is to improve the interface quality. Over the past few years, various pre-gate surface passivation techniques have been developed to improve the high-k/Ge interface quality and recently, GeO_2 as a native oxide layer, formed by either thermally grown [2], rf-sputtering [3, 4], ozone oxidation [5], or atomic layer deposition (ALD) [6], is of particularly interest as it may be the most nature material to passivate Ge surface. Good interface quality with low interface trap density [2, 5] or highest recorded hole mobility [3] have been reported. However, few post gate dielectric (post-gate) treatments have been studied for Ge devices. Forming gas annealing (FGA) may be one choice. However, some studies report that FGA can reduce the interface states for Ge [7] whereas other studies suggest that passivation of Ge dangling bonds by hydrogen is ineffective [8]. Moreover, though the pre-gate surface passivation treatments can offer a good interface quality, due to the lower processing temperature for Ge devices, there are still significant bulk defects in high-k dielectrics, especially near high-k/Ge interface (usually a PDA of ~700°C is used to repair these defects for high-k/Si stack) and these defects may be the cause for mobility degradation and bias temperature instability. Thus a post-gate treatment with lower thermal budget is highly desired. Recently, an alternative post-gate passivation by fluorine (F) incorporation into high-k/Ge gate stack has been reported [9]. It has been shown that F can segregate near high-k/Ge interface and reduce both interface states and high-k bulk traps. In this study, for the first time, we investigate the effects of F incorporation into high-k/Ge gate stack with GeO_2 passivation, as well as the combination effects of both F incorporation and FGA.

2. Experiment

The starting wafers were n-type Ge wafers (Sb doped, R= 0.13-0.14Ωcm). The native oxide was removed by a cyclic rinsing between deionized water and diluted HF. A thin Ge oxide layer about 2 nm was then thermally grown on germanium substrates at 400°C, followed by an HfO_2 layer of 4.5 nm deposited using ALD. After the gate dielectric deposition, fluorine was introduced into some samples using CF_4 plasma treatment as described in [9] (Fig. 1) with different treatment durations. Post deposition annealing was then performed for all samples at 500°C in N_2 ambient for 30s. After that, a 150 nm TaN gate electrode was then sputtered, followed by lithography and dry etching. A 100 nm Al was deposited on the bottom of Ge substrates for the ohmic contact and finally forming gas annealing (FGA) at 350°C for 1 hour was performed for some samples.

3. Results and Discussion

Fig. 2 shows the angle resolved XPS Ge 3d spectra for Ge samples after thin germanium oxide growth. The difference in binding energy of oxide and substrate peaks is 3.3 eV for both 30° and 90° takeoff angle, indicating Ge^{4+} is present at both surface of GeO_2 and near the GeO_2/Ge interface [10]. No significant components of germanium suboxides were detected. Fig. 3 shows the *C-V* frequency dispersion characteristics of TaN/HfO_2/GeO_2/Ge MOS capacitors without FGA. For the samples without CF_4 treatment [Fig. 3(a)], kinks are clearly visible below 100 kHz and a frequency dependent flat band voltage shift (ΔV) about 200 mV is observed, which is the direct result of interface states. Particularly for the PMOS capacitors, ΔV is the indication of high D_{it} in the upper half of Ge bandgap [9]. For the samples with CF_4 treatment for 3 min [Fig. 3(b)], both ΔV and size of the kinks become much smaller. Good *C-V* shapes with various frequencies have been achieved. This is attributed to reduced interface states and bulk traps through the F incorporation. Fig. 4 shows the *C-V* frequency dispersion characteristics for samples with FGA. It can be seen that ΔV and size of kinks are reduced for both samples with and without CF_4 treatment. *C-V* stretch-out becomes smaller and almost diminishes for samples with 3 min CF_4 treatment.

EOT values were extracted by fitting the *C-V* data using lower frequency curves (10 kHz) in accumulation which are the least affected by series or shunt resistance [11] and are summarized in Fig 5. It can be seen that F incorporation will not cause any significant EOT change (~ 1 Å EOT increment). The decrease of EOT values (~ 1.5 Å) after FGA is due to the high-k densification. The total EOT value is about 1.6 to 1.7 nm for HfO_2/GeO_2 dual layer. This leads to an EOT contribution of ~ 0.8 nm from GeO_2 assuming EOT contribution is ~ 0.9 nm for 4.5 nm HfO_2. The relative dielectric constant of GeO_2 is thus about 9.8, which is consistent with value (~ 7 to 12) reported in [1]. Further, frequency dependent flat band voltage shifts are summarized in Fig. 6 for samples of different F treatment conditions with or without FGA. A great reduction of ΔV is observed after 1 min CF_4 treatment and ΔV diminishes after FGA for samples with 2 or 3 min CF_4 treatment. Gate leakage current is shown in Fig. 7. Low leakage currents of order of 10^{-7} to 10^{-6} A/cm^2 are observed for all the samples, indicating good gate dielectrics (HfO_2/GeO_2 dual layer) quality. Samples with F incorporation show smaller leakage current. This is possibly due to lower trap assisted tunneling. It should also be noted that samples with F incorporation have about 1 Å thicker EOT. Finally, D_{it} was measured using frequency dependent conductance method. Fig. 8 shows the typical measured frequency dependencies of G_p/ω for various gate voltages for samples with FGA. The inset is the plot of the extracted D_{it} values at midgap. A low D_{it} value of 6.33×10^{11} cm^{-2}eV^{-1} is observed for samples without CF_4 treatment and D_{it} further decreases as CF_4 treatment duration increases. D_{it} value as low as 2.02×10^{11} cm^{-2}eV^{-1} is achieved for samples with 3 min CF_4 treatment, approaching state-of-the-art metal-gate/HfO_2/SiO_2/Si gate stacks (typically mid to high 10^{10} cm^{-2}eV^{-1}).

4. Conclusion

A post-gate passivation technique using CF_4-plasma treatment on Ge gate stack has been proposed. F incorporation improves electrical characteristics like frequency dispersion, *C-V* stretch-out and reduces interface trap densities. The effect of FGA has also been investigated. It was found that interface quality can be further improved by combining FGA and F incorporation. High-k/Ge MOS capacitors exhibiting excellent electronic properties with minimum D_{it} as low as 2.02×10^{11} cm^{-2}eV^{-1} has been demonstrated through the pre-gate GeO_2 passivation, post-gate F incorporation and FGA. Proper post-gate treatment offers a new route to further optimize high-k/Ge interface quality.

References

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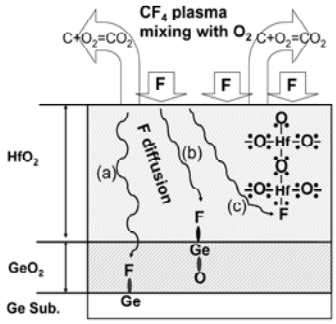

Fig. 1. F incorporation into high-k/Ge gate stack and various possible passivation mechanisms during subsequent annealing steps: (a) passivation of interface traps at GeO_2/Ge interface; (b) passivation of interface traps at HfO_2/GeO_2 interface; (c) passivation of HfO_2 bulk traps.

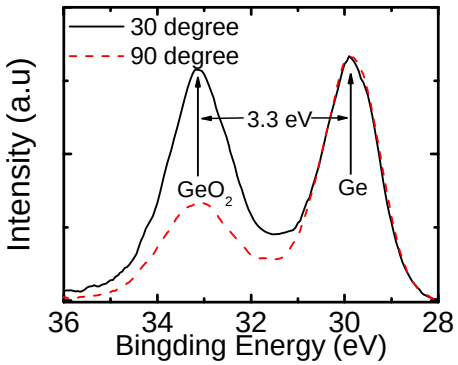

Fig. 2. Angle resolved XPS Ge 3d spectra for germanium samples after the thermal oxidation at 400°C. The thickness of GeO_2 is about 2 nm.

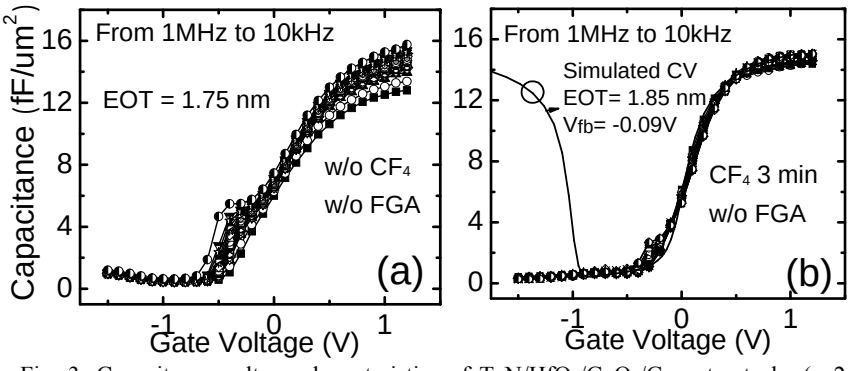

Fig. 3. Capacitance-voltage characteristics of TaN/HfO_2/GeO_2/Ge gate stacks (~ 2 nm GeO_2 and 4.5 nm HfO_2) without FGA measured at 1Mhz, 900kHz, 800kHz,…, 200kHz, 100kHz, 90kHz, 80kHz,…, 20kHz and 10kHz (a) without CF_4 plasma treatment and (b) with CF_4 plasma treatment for 3 min.

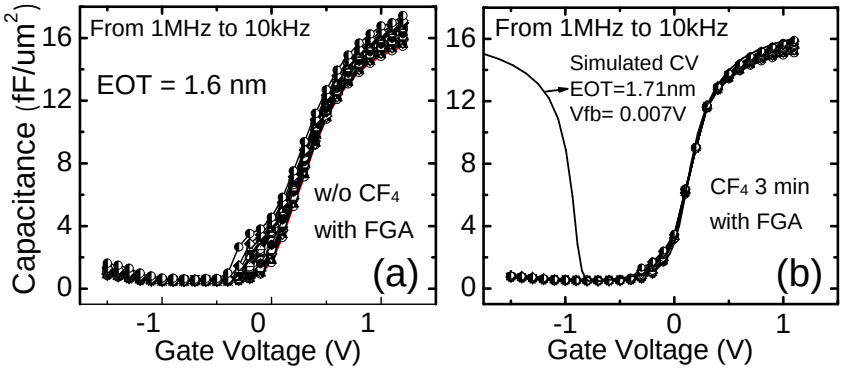

Fig. 4. Capacitance-voltage characteristics of TaN/HfO_2/GeO_2/Ge gate stacks (~ 2 nm GeO_2 and 4.5 nm HfO_2) with FGA at 350°C for 1 hour measured at 1Mhz, 900kHz, 800kHz,…, 200kHz, 100kHz, 90kHz, 80kHz,…, 20kHz and 10kHz (a) without CF_4 plasma treatment and (b) with CF_4 plasma treatment for 3 min.

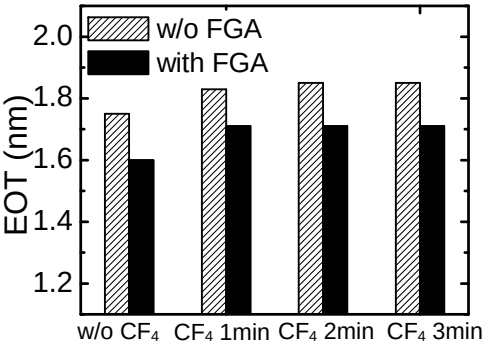

Fig. 5. Equivalent oxide thickness (EOT) for samples both with and without FGA of different CF_4 treatment conditions.

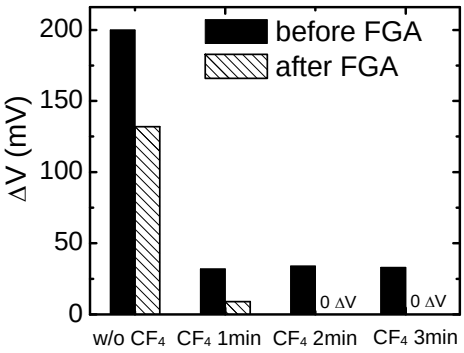

Fig. 6. Frequency dependent flat band voltage shifts (ΔV) for samples both with and without FGA of different CF_4 treatment conditions.

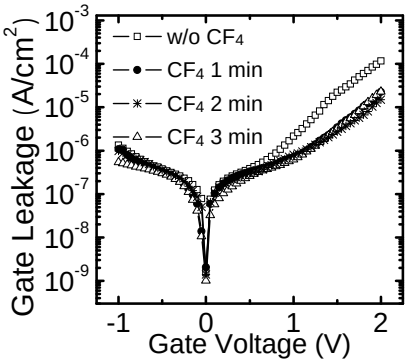

Fig. 7. I_g-V_g characteristics for forming gas annealed samples with different CF_4 plasma treatment conditions.

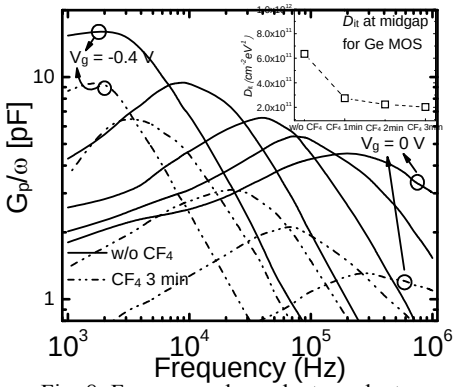

Fig. 8. Frequency dependent conductance G_p/ω for a series of gate voltage for forming gas annealed samples without CF_4 plasma treatment and samples with CF_4 plasma treatment for 3 min. Inset is the extracted midgap D_{it}.