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Improvement of Interface Properties of GeO_2/Ge MOS Structures Fabricated by Thermal Oxidation

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1. Introduction

Ge-channel MOSFETs have been proposed as a promising candidate of future device structures over the scaling limit of Si technology, because of the higher carrier mobility than Si. On the other hand, the realization of the superior MIS interfaces is one of the most critical issues for establishing Ge MOS technology. It has recently been reported that the interface state density (D_{it}) of GeO_2/Ge interfaces is one of the lowest level among a variety of Ge MIS interfaces [1-3] and also that GeO_2/Ge interfaces can works as a good interface layer between Ge-channel and high-k insulators [4]. However, the Ge MIS interfaces reported so far [1-4] have been fabricated by low temperature processes and the effects of the oxidation temperature and the surface orientation on the MIS interface properties have not been studied yet. Also, the quantitative analyses on the energy distribution of D_{it}, which are quite important in understanding the impact on CMOS performance as well as the physical origin of D_{it}, have not been fully evaluated yet.

In this paper, the electrical properties of GeO_2/Ge MIS interfaces fabricated by thermal oxidation of Ge substrates are quantitatively evaluated. We fabricate GeO_2/Ge MIS structures by various temperature conditions and evaluate the energy distribution of D_{it} by the low temperature conductance method. Furthermore, we examine the effects of the surface orientation and annealing before/after forming metal electrodes in atmospheres of various gases on MIS interface properties.

2. Samples Fabrication

GeO_2/Ge capacitors were fabricated on (100), (110) and (111) oriented n- and p- type Ge substrates. Cyclic HF dip with DI water was used to remove Ge native oxides before the thermal oxidation. Subsequently, GeO_2 was formed by thermal oxidation at temperatures from 450°C to 600°C. Finally, Al films were deposited to form gate electrodes. For evaluating D_{it} and the energy distribution, we used the low temperature conductance method considering in surface potential fluctuation [5, 6]. The temperatures from 80K to 150K were used. We have already reported that this method allows us to evaluate D_{it} in a wide range of surface potential [6].

3. Results and Discussions

Fig. 1 shows C-V characteristics of GeO_2/(100)n-Ge capacitors oxidized at 550°C at measurement temperatures of RT and 100K. While the frequency dispersion attributed to the minority career response is observed at RT, superior C-V curves, free from frequency dispersion, are found to be obtained at 100K. Fig.2 shows the energy distribution of D_{it} of GeO_2/(100)Ge capacitors fabricated by thermal oxidation at temperatures from 450°C to 575°C. It is found that the D_{it} distributions are in the U shape, as similar with Si MOS interfaces, and the amount of D_{it} decreases systematically as the oxidation temperature increases. The detected minimum D_{it} values for MOS capacitors fabricated at 575°C, obtained near the midgap, are 9.3×10^{10} and 1.1×10^{11} $eV^{-1}cm^{-2}$ in the conduction band and the valence band side, respectively, which is almost in the same low level as in thermal oxidation SiO_2/Si interfaces. It is also found in Fig.3 that the densities of oxide fixed charges, estimated from V_{FB} shift, and slow trap charges, estimated by hysteresis, have the same tendency to decrease with an increase in the oxidation temperature. On the other hand, MOS capacitors oxidized at 600℃ had very rough surfaces and did not exhibit normal C-V characteristics. It can be concluded from these results that, from the viewpoint of reduction in interface defect density, the oxidation temperature should be as high as possible within the temperature range where the surface roughness due to GeO volatilization can be suppressed.

Fig.4 shows the energy distribution of GeO_2/Ge on (100), (110) and (111) surfaces oxidized at 450°C and 550°C. It is found that the amount and the energy distribution of D_{it} on (110) and (111) surfaces are same as those on (100) and the values of detected minimum D_{it} are also around 1×10^{11} $eV^{-1}cm^{-2}$. These results suggest that GeO_2/Ge interfaces have no surface orientation dependence of D_{it}, which is quite different from SiO_2/Si interfaces.

In order to further reduce D_{it}, annealing before or after metal gate formation were carried out by using N_2, H_2, and atomic hydrogen. It is found in Fig. 5 that the atomic hydrogen annealing before Al gate formation at 200°C or higher leads to further decrease D_{it} down to less than 7.5×10^{10} $eV^{-1}cm^{-2}$ in conduction band side and less than 9.3×10^{10} $eV^{-1}cm^{-2}$ in valence band side respectively. On the other hand, the annealing after Al gate formation has caused the increase in D_{it}, irrespective of the gas atmospheres, attributable to the deterioration associated with any reaction between Al and Ge oxides. It is concluded, as a result, that the atomic hydrogen annealing before Al gate deposition is effective in hydrogen passivation with GeO_2/Ge MOS interface defects.

4. Conclusion

The interface properties of GeO_2/Ge MIS structures fabricated by thermal oxidation were quantitatively evaluated. It has been found that D_{it} in GeO_2/Ge MOS

interface systematically decreases with an increase in the oxidation temperature and that the detected minimum D_{it} becomes lower than 1×10^{11} $eV^{-1}cm^{-2}$ in case of the oxidation at 575°C. Different from SiO_2/Si, GeO_2/Ge has no surface orientation dependence of D_{it}, while the energy distribution is almost the U shape like SiO_2/Si. It is also found that atomic hydrogen annealing before Al deposition can further reduce D_{it}.

References [1] S. Takagi et al., Microelectron. Eng. 84 (2007) 2314 [2] T. Takahashi et al., IEDM (2007) 697 [3] A. Delabie et al., APL (2007) 91, 082904 [4] D. Kuzum et al., IEDM (2007) 723 [5] J. R. Brews et al., Solid State Electron., 26 (1983) 711 [6] H. Matsubara et al,, SSDM (2007) 18

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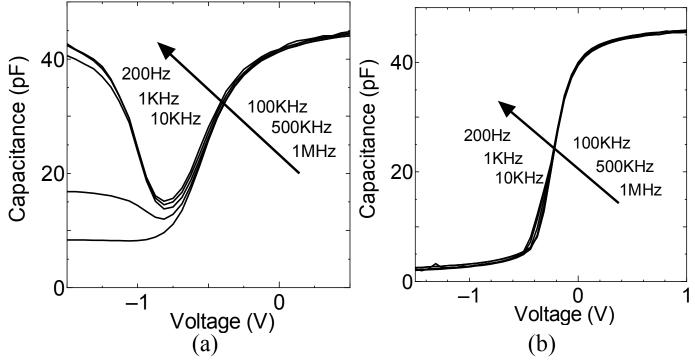

Fig.1 C-V characteristics of GeO_2/(100)Ge capacitors oxidized at 550°C. The measurement temperature is (a) R.T. (b) 100K.

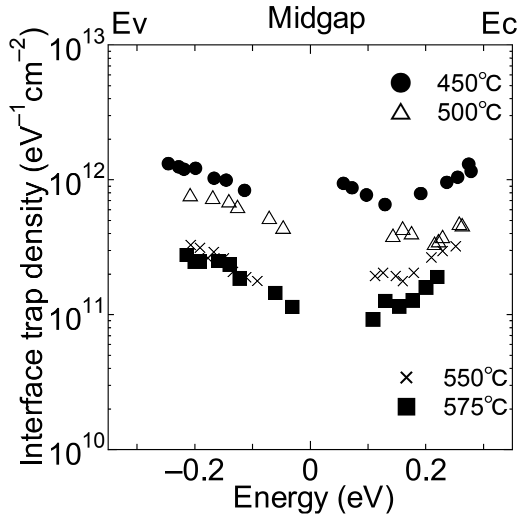

Fig.2 Energy distribution of interface state densities of GeO_2/(100)Ge capacitors oxidized at 450°C, 500°C, 550°C and 575°C. The D_{it} measurement was performed by the conductance method.

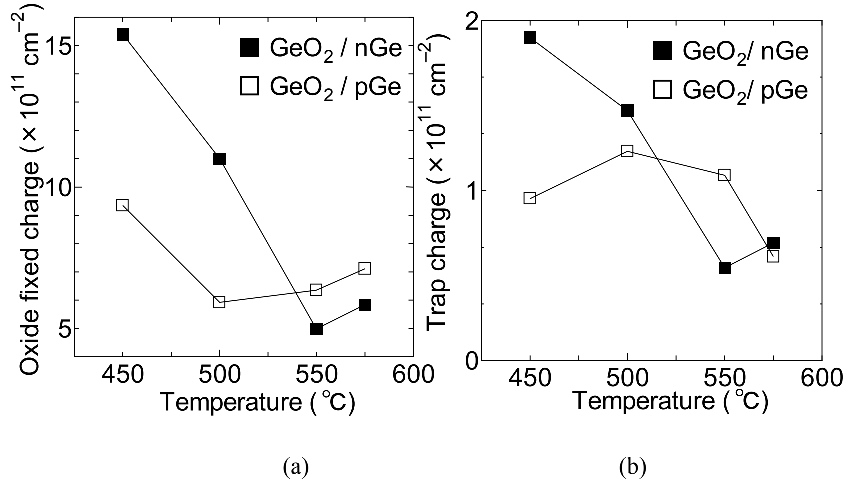

Fig.3 Oxidation temperature dependence of (a) oxide fixed charge (b) slow trap charge density in GeO_2/(100)Ge capacitors

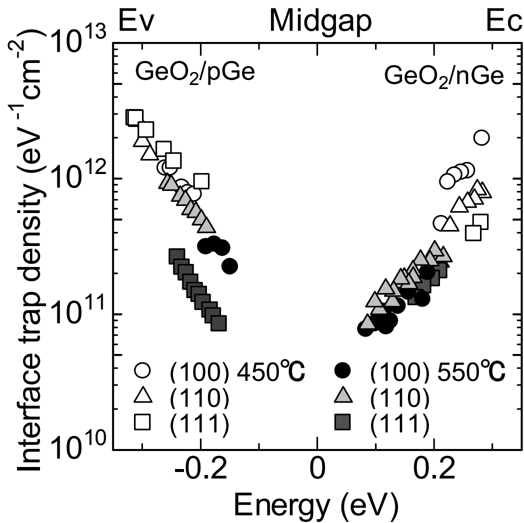

Fig.4 Energy distribution of interface state densities of GeO_2/Ge(100), (110) and (111) oxidized at 450°C and 550°C.

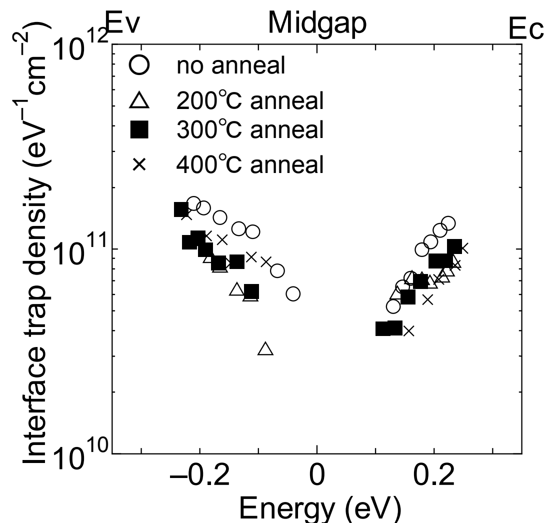

Fig.5 Comparison of D_{it} of GeO_2/(100)Ge capacitors oxidized at 550°C after annealing by atomic hydrogen before Al gate deposition as a parameter of annealing temperature.