Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 18-19

A-2-1 (Invited)

Performance and reliability of high-k/metal gate stacks: Interfacial layer defects

Gennadi Bersuker

SEMATECH, 2706 Montopolis Dr., Austin TX 78741
Phone: 512-356-7045; gennadi.bersuker@sematech.org

1. Introduction

High-k/metal gate stacks were recently introduced into CMOS technology for the 45 nm node and beyond. While employing high-k dielectrics has many advantages, such a drastic modification of the CMOS process introduces a number of challenges. High-k gate stacks are multilayer structures that include a SiO_2 layer (IL) at the high-k film interface with the Si substrate. The high-k dielectric and IL are subject to intermaterial interactions between themselves and with the metal electrode. This interaction, which is strongly assisted by the high temperature processing of transistors, creates additional structural defects in the IL. These defects may impact the electrical properties of the gate stacks and engender a whole spectrum of new performance and reliability phenomena. For instance, Hf atoms that diffuse into the IL have been suggested to be responsible for the fast component in negative bias temperature instability (NBTI) measurements [1]. Oxygen deficiency in the IL, which is induced by the combined influence of both the high-k dielectric and metal electrode [2], results in a perceived instability of the metal electrode work function and controls stress-induced gate stack degradation and breakdown. Below we focus on several important and seemingly different manifestations of instability—NBTI, gate stack degradation under constant voltage stress, and instability of the effective work function in p-type devices—and will show that these phenomena are controlled by defects in the interfacial SiO_2 layer, a "weak link" in high-k/metal gate stacks.

2. NBTI

Negative bias temperature instability (NBTI) represents one of the major concerns in MOSFET reliability and has been shown to play a dominant role in scaled high-k dielectrics. Reported results [1,3] suggest that the IL is largely responsible for NBTI in the high-k gate stacks. However, certain NBTI features were found to be quite different from those in conventional SiO_2 gate dielectrics due to modifications to the IL composition induced by its interaction with the overlaying high-k film [2]. High-k and SiO_2 gate stacks show a similar long-term growth rate of stress-generated interface traps, $\Delta V_{TH} \propto t^n$, n ≈0.2, as monitored by the DCIV technique, Fig.1. However, for short stress times (<1s), additional fast interface trap generation has been observed in high-k gate stacks, which could originate from the as-processed precursor defects. Spin dependent recombination (SDR) measurements [1] indicate that this fast interface trap generation could be associated with defects related to the Hf atoms, the density in IL of which was found to be on the order of 10^{12}–10^{13}cm^{-2} [2]. To separate the fast trap generation process from a slow one, which is responsible for long-term ΔV_{TH} degradation, an analysis is proposed in which the contribution of the fast transient trap generation process is approximated by the ΔV_{TH} value after the first 1s of stress ΔV_{TH} (1s). The slow, conventional, interface trap generation is then obtained by subtracting ΔV_{TH} (1s) from the measured ΔV_{TH} (t) dependence, Fig.1. This procedure results in physically correct kinetics of the defect generation in the high-k gate stacks, which is similar to SiO_2.

3. Constant voltage stress

In all cases of the inversion constant voltage stress (CVS), the stress-induced leakage current (SILC) strongly correlates to the evolution of the gate current degradation features, e.g., soft breakdown (BD), progressive BD, and hard BD, during CVS [4]. This indicates that the dielectric layer controlling SILC growth is the major contributor to the dielectric stack degradation, thus representing the "weak link" in the high-k gate stack. On the other hand, similar growth rates for SILC and interface trap density (N_{it},) observed for each gate stack of a given high-k thickness, Fig.2, indicate that their growth is most likely driven by the same underlying physical cause (i.e., by the same defects). Since the N_{it} stress time dependency is similar for charge pumping (CP) with high and low frequencies, which probes traps near the interface with the Si substrate and deeper in the IL, respectively, one may conclude that the N_{it} values correspond to the traps generated primarily within IL. This conclusion is supported by the simulation of the CP probing depth [5], which, under the conditions used for these CP

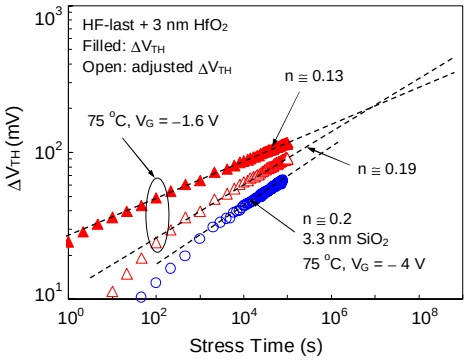

Fig.1 Measured (filled triangles) and adjusted for fast transient (open triangles) V_{TH} shift vs. stress time. The open circles show V_{TH} shift for reference SiO_2 device.

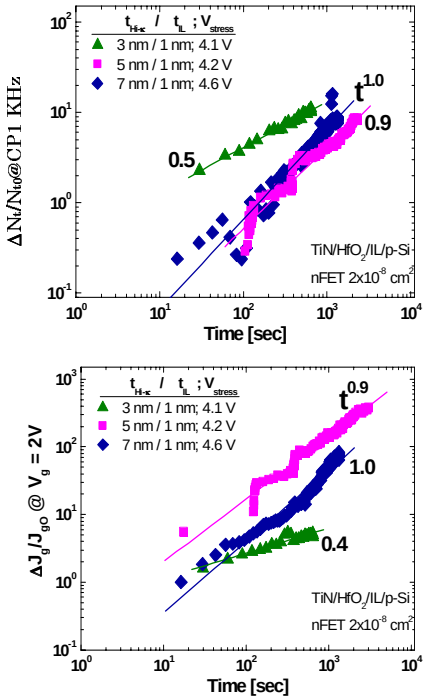

Fig. 2 SILC (a) and N_{it} (b) growth rates in the 3 nm, 5nm, and 7nm HfO_2 gate stacks. Similar SILC and N_{it} slopes are observed for each HK thickness

measurements, was estimated to lie within the IL. High-k dielectrics can form Si-Si defects in the IL (by generating oxygen vacancies), which could be converted into electron traps (by breaking the Si-Si bonds) during stress. On the other hand, high-k metal-insulator-metal (MIM) samples, which had no IL, showed negligible SILC. Therefore, the strong correlation of SILC to N_{it}, as well as gate current simulations, which include trap-assisted tunneling, suggests that SILC and hence breakdown are mostly triggered by IL degradation.

4. Flatband voltage roll-off

It has been reported that when metal/high-k gate stacks were used in devices of practical interest, with scaled down equivalent oxide thicknesses (EOTs), their effective work function (EWF) values were significantly reduced with respect to those obtained in the test structures with thicker gate stacks, most drastically in the cases of gate stacks with high EWFs (P-type electrodes) [6]. This phenomenon, which significantly limits the available options for metal/high-k transistor fabrication, is called flatband voltage (V_{fb}) roll-off (R-O).

We propose a model suggesting that the R-O phenomenon is caused by enhanced positive charge generation in the interfacial SiO_2 layer. Ab initio calculations demonstrate that a positive charge can be generated in the IL when it is sufficiently thin so that the HfO_2-induced oxygen out-diffusion occurs from the SiO_2 layer next to the interface with the Si substrate [7].

Physical, electrical, and modeling data support the premises of the proposed R-O model. Indeed, thicker

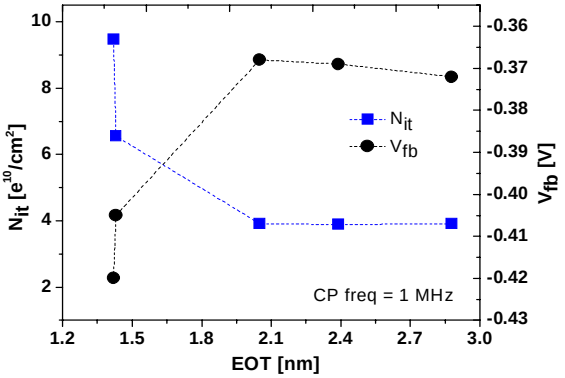

Fig. 3 Correlation between V_{fb} and interface trap density N_{it} measured on the HfO_2/TiN transistors fabricated using the terraced oxide structure.

high-k films (up to a certain thickness value defined by the diffusion length of the vacancies under the given process conditions) function as a stronger oxygen vacancies source for the interfacial SiO_2 layer leading to greater R-O. Similarly, higher WF electrodes, which exhibit higher efficiency in generating oxygen vacancies in transition metal oxides, are expected to enhance R-O by increasing oxygen vacancy supply (via the higher-k film) to the interfacial oxide. Both generation and diffusion of oxygen vacancies in the dielectric stacks are controlled by the thermal budget leading to a strong R-O temperature dependency. Since the charge state of the oxygen vacancies in the interfacial SiO_2 layer depend on the position of the substrate Fermi level, the probability for the vacancy to be in a positive charge state (rather than neutral) increases in the gate stack fabricated with the p-Si that explains the R-O dependence on the substrate type. HfO_2/TiN pMOS transistors fabricated on the terraced oxide structures [8] with varying SiO_2 thicknesses from 0–8 nm demonstrate a strong correlation between the V_{fb} roll-off and interface state density N_{it} (extracted using CP techniques) measured on the same devices, Fig. 3. These data support the model assumption that roll-off is caused by the oxygen deficiency of the SiO_2 near the Si interface.

5. Summary

The above examples demonstrate that the metal/high-k-induced oxygen vacancies in the IL are responsible for a variety of performance and reliability degradation phenomena. They implicate the interfacial layer as the gate stack "weak link," process control over which properties, in particular stochiometry, can help to meet dielectric scaling requirements.

References

[1] A. Neugroschel et al., IEDM Proc., (2006) 317.
[2] G. Bersuker et al., J. Appl. Phys. **100** (2006) 094108.
[3] A. Neugroschel et al., IEEE TDMR **8** (2008) 47.
[4] G. Bersuker et al., IRPS Proc. (2007) 49.
[5] D. Heh et al., IEEE TED **54** (2007) 1338
[6] B. H. Lee et al., Materials Today **9** (2006) 36
[7] G. Bersuker et al., ESSDERC Proc. (2008)
[8] G. A. Brown et al., Ext. abstracts of SISC (2004) 15