Impact of the Activation Annealing Temperature on the Performance, NBTI and TDDB lifetime of High-k/Metal gate stack pMOSFETs

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Abstract
We have clarified the impact of the activation annealing temperature on the NBTI and TDDB lifetime improvement of HfSiON / TiN gate stack pMOSFETs. Higher temperature annealing is effective for the NBTI and TDDB lifetime improvement. This is due to the Si substrate oxidation during the high temperature anneal resulting in the interface defect state reduction. And it is also effective for Vth reduction following device performance improvement.

Introduction
High-k / metal gate stacks are now ready for production. Thus, the focus for discussion is moving to the reliability problems. Among the many reliability items, NBTI and TDDB are one of the most serious problems for high-k/metal pMOSFETs. There are many reports regarding the NBTI degradation [1-3] and breakdown mechanisms [4] and its reliability improvement techniques. However, the mechanisms are still open to question. Furthermore, more investigation is required for the fabrication of highly reliable pMOSFETs. In this study we have investigated the impact of the activation annealing temperature on the NBTI and TDDB lifetime for High-k/Metal gate stack pMOSFETs.

Experimental
Following HfSiO MOCVD, nitrogen atoms were incorporated into HfSiO by plasma nitridation to form HfSiON. TiN, for gate electrodes was deposited by PVD. Source and drain activation annealing temperatures were varied at from 1015 to 1100°C as shown in Table I. To evaluate the reliability characteristics, charge pumping, NBTI and TDDB were measured for pMOSFETs in inversion states at 125°C.

Results and Discussion

Initial electrical characteristics
Fig. 1 shows the values of EOT of the samples. With increasing RTA temperature, EOT values were slightly increased (~0.06nm). Also with increasing RTA temperature, Vth reduction of pMOSFETs was observed as shown in Fig. 2 (~80mV). Furthermore, hole mobility in pMOS was improved with higher temperature annealing (Fig.3). As an effect of both Vth reduction and mobility improvement, Ion of pMOSFETs was increased by about 35% (Ioff = 10^-7 A/µm) (Fig. 4). Higher temperature annealing was effective for pMOSFETs device performance improvement. Fig. 5 shows the charge pumping current (Icp) as a function of base bias (f=500 kHz, Vbias = -1 V). It clearly shows that, with increasing RTA temperature, interface state densities were reduced. It was clarified that high temperature RTA was effective for the improvement in interface state conditions.

NBTI
Fig. 6 shows the time evolution of ΔVth in NBTI (125°C, Vstress=Vth-1.2 V). It clearly shows that higher temperature anneals cause ΔVth reduction. To clarify the improvement mechanism, we have measured the stress & charge pumping technique to analyze the interface state degradation phenomena under bias temperature stress. Fig. 7 shows Icp as a function of Vbias of sample C. With increasing stress time, it can be observed that interface state densities were increased. It is thought that NBTI degradation was basically due to the interface state density increase as a result of hydrogen de-passivation [2,3,5]. That indicated that the NBTI improvement with higher temperature annealing was based on an interface state condition improvement.

TDDB
Fig. 9 shows the tentative Ig-t characteristics of a pMOSFET in the inversion state (sample C). We can observe an abrupt gate leakage jump (hard breakdown) without progressive breakdown. Thus, we could determine easily the time to breakdown (Tbd). Fig. 10 shows the Weibull distribution of Tbd of the evaluated samples. It clearly shows that a higher RTA temperature is effective in improving TDDB lifetime. Lifetime improvements were observed at any bias (Fig. 11). It has been reported that TDDB lifetime of pMOS in the inversion states, was determined by cathode electron injection and there is a common relationship between Tbd and cathode injection electron current in case of the same physical HfSiON thickness [4]. Fig. 12 shows the cathode injection electron current, measured using carrier separation technique as a function of gate bias. With increasing RTA temperature, electron currents were suppressed. And there was common relationship between TDDB lifetime and cathode injection electron in this case, as noted in our previous report [4]. This means that the HfSiON, itself, maintained the same physical thickness and characteristics for breakdown. We can conclude that TDDB lifetime improvement was due to the suppression of cathode injection electrons due to a slight increase in the interface layer.

Effect of high temperature annealing
Considering the interface state improvement in NBTI with a slight EOT increase, it is thought that high temperature annealing causes Si substrate oxidation (Fig. 13), consequently reducing the interface state defects leading to reliability improvement. This oxidation is also effective in reducing Vth with the very slight EOT increase (~0.06 nm).

Conclusion
We have clarified that higher temperature annealing is effective for device performance, NBTI and TDDB lifetime improvement of HfSiON / TiN gate stack pMOSFETs. The improvement mechanism is based on the Si substrate oxidation to obtain a high quality interface during the higher temperature annealing.

References
Table I RTA conditions evaluated in this study.

<table>
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<tr>
<th>RTA Temp. (°C)</th>
<th>A 1015</th>
<th>B 1050</th>
<th>C 1100</th>
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<tbody>
<tr>
<td>EOT (m)</td>
<td>0.85</td>
<td>0.85</td>
<td>0.95</td>
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Fig. 1 EOT of the samples. (using CVC) RTA causes a slight EOT increase.

Fig. 2 Vth as a function of gate length of pMOSFETs. Higher temperature RTA is effective for Vth reduction.

Fig. 3 Hole mobilities as a function of E_{eff}. With RTA temperature increase, mobilities were increased.

Fig. 4 Ion-Ioff characteristics of pMOSFETs. With the effect of higher temperature RTA, Ion was increased.

Fig. 5 Charge pumping current as a function of V_{th}. With RTA temperature increase, Dit values were decreased.

Fig. 6 Time evolution of ΔV_{th} in NBTI. With RTA temperature increase, ΔV_{th} were suppressed.

Fig. 7 Charge pumping current as a function of V_{th}. Values were suppressed.

Fig. 8 Time evolution of ΔN_i. With RTA temperature increase, ΔN_i were suppressed.

Fig. 9 lg-t characteristics of Sample B. Abrupt gate leakage current jumps were observed.

Fig. 10 Weibull distribution of T_{bd} of HfSiON. With RTA temperature increase, T_{bd} were increased.

Fig. 11 T_{bd} as a function of overdrive stress voltage. With RTA temperature increase, T_{DDDB} lifetimes were increased.

Fig. 12 Cathode injection electron as a function of gate bias. With RTA temperature increase, electron currents were suppressed.

Fig. 13 T_{bd} as a function of cathode injection electron. There exist a common relationship between T_{bd} and I_{el}.

Fig. 14 Schematic of high temperature annealing. Oxygen in HfSiON oxidized Si substrate during RTA.

<table>
<thead>
<tr>
<th>Icp (A)</th>
<th>10^{-8}</th>
<th>10^{-8}</th>
<th>10^{-8}</th>
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<th>10^{-8}</th>
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<tr>
<td>Tbd (s) @ 63% Failure</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
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</tbody>
</table>

With RTA temperature increase, electron lifetimes were increased.

Temperature increase, electron lifetimes were increased. With RTA temperature increase, electron lifetimes were increased.

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V_{th} in NBTI.

Hole mobility (cm²/Vs).

Interface growth.

RTA Si-sub.