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Mechanisms of oxygen and hydrogen passivation using high pressure post-annealing processes to enhance the performance of MOSFETs with metal gate/high-k dielectric

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Abstract: Novel high pressure oxygen anneal (HPOA) and high pressure hydrogen anneal (HPHA) processes have been developed to achieve high effective work function (EWF) (>5.2eV) for pMOSFETs and to form a high quality interface, simultaneously. An EWF boost of 500meV was achieved using the HPOA without EOT increase. After the HPHA, interface states were reduced by 30%, which resulted in an improved the transconductance (G_m) and on current (I_{on}). Mechanisms for these improvements are discussed to guide future process optimizations.

Introduction

An effective workfunction modulation for pMOSFETs and the proper interface passivation have been challenging for MOSFETs with metal electrode/high-k dielectric stacks [1]. A conventional forming gas anneal (FGA) process using diluted hydrogen was found to reduce the oxygen-rich metal electrode, resulting in a lower EWF for pMOSFETs, and a higher FGA temperature was required to passivate the high-k/Si interface, which may degrade Ni silicide [2].

In this work, a high pressure FGA using O_2 and H_2 ambient was applied to enhance the EWF of pMOSFETs to >5.2eV and to efficiently passivate the interface states while keeping the process temperature below 400°C to avoid additional process-induced defects. Different diffusion paths were identified for these passivation gases, and optimal materials are proposed to maximize the benefits of high pressure annealing.

Experiment

For the HPHA, the presence of nitride retarding the diffusion of hydrogen is a concern. In this case, 3nm HfON films were deposited using ALD, followed by post-deposition annealing in NH_3 ambient. Then, a 10nm ALD TiN/100nm poly-Si electrode stack was deposited. To exclude silicide-induced stress effects, the silicidation process was omitted. To study the effect of the contact etch stop layer (CESL), three different plasma-enhanced chemical vapor deposition (PECVD) nitride stress layers (tensile, control, and compressive) were used in both nMOSFET and pMOSFET devices. Also, high temperature rapid thermal CVD nitrides were used to investigate the interface passivation mechanism. After a standard FGA, HPHA was performed at 10atm.

For the HPOA, terraced oxide PMOS capacitors and both gate-first and gate-last pMOS transistors were fabricated on an N-type Si substrate as shown in Fig. 1-(b) [3,4]. To demonstrate the sensitivity to oxygen ambiment, RuO_2 electrode was chosen. Two integration schemes with and without a high temperature source/drain (S/D) activation anneal (>1000ºC) were used to investigate the impact of the heat cycle. At the end of the process flow, an atmospheric pressure oxygen anneal (APOA) or HPOA at 10atm was applied.

The post-high pressure anneals were performed using an in-house 200mm/300mm very high pressure (VHP) chamber manufactured by Poongsan Microtech USA.

RESULTS AND DISCUSSION

1. High Pressure Hydrogen Anneal (HPHA)

Stress in the nitride film can be modulated by changing a relative share of the Si-H and Si-N bonding [6, 7]. The improvement in I_{on} for the nMOS with the tensile stressor CESL is ~12%, indicating the impact of process split (Fig. 2). For the tensile stress nitride layer, Si-H is the preferred bonding. On the other hand, Si-N bonding dominates in compressive film. In the compressive stressor, therefore, extra hydrogen can diffuse into the channel region and passivate dangling bonds at the interface with Si, which in turn decreases the interface state density D_{it} (Fig. 3-(a)). After the HPHA, the interface states were significantly reduced for all the CESL structures (Fig. 3-(a)). Due to its excess hydrogen before the HPHA, the compressive CESL exhibited the lowest ΔI_{cp}, which resulted in less of a G_{mmax} improvement as shown in Fig. 3-(b). After the HPHA, a 5.4% improvement in I_{on} was observed for the tensile CESL devices due to maximized interface passivation effects (Fig. 4). According to ΔG_{mmax} and ΔI_{on}, there was no stress relaxation regardless of stressor nitrides even after the HPHA.

The difference in D_{it} before and after HPHA, ΔI_{cp}, for the RTCVD CESL samples was negligible while PECVD samples showed greater G_{mmax} improvement (Fig. 5-(a)). This result can be explained by the lower thermal budget for PECVD nitride during film deposition and process-induced damage due to the plasma process. The RTCVD nitrides were deposited at a higher temperature (>750ºC). Thus, Gmmax and I_{on} improvements were less significant due to less hydrogen passivation through the RTCVD nitride layer (Fig. 6 and 7). However, I_{cp}, G_{mmax}, and I_{on} did not degrade even for the RTCVD devices. For both SiN methods, the improvement in the device parameters was less with thicker SiN due to less hydrogen diffusion. These results suggest that hydrogen diffuses through the ILD and CESL rather than through the gate stacks and an RTCVD nitride can mitigate post-hydrogen passivation. In CMOS integration, however, this RTCVD nitride cannot easily implemented because of its high thermal budget (Fig.13).

2. High Pressure Oxygen Anneal (HPOA)

Even with a low temperature APOA, the EWF boost ~200mV was demonstrated a as shown in Fig. 8. This EWF boost is attributed to the partial elimination of O vacancies in the high-k [3] and/or the stoichiometric stabilization of Ru oxide (i.e., RuO_2) caused by adding oxygen to the Ru oxide and/or Ru oxide/high-k interface from the APOA process. According to secondary ion mass spectroscopy (SIMS) analysis, the low temperature oxygen anneal process increased the oxygen content in TaN, Ru oxide, and the Ru oxide/high-k interface (Fig. 9)[2]. Therefore, a HPOA is expected to be able to control the oxygen content more efficiently due to higher solubility (Henry's Law) in the metal lines and enhanced diffusion [5]. Fig.10 shows that the HPOA enhances the EWF with a minimal impact on EOT at an optimized O_2 concentration. For full metal gate stack, both gate first electrode and gate last electrode showed an apparent EWF change around 500mV while the HPOA seems not effective with a polysilicon gate capping (Fig. 11, 12). The fact that the FGA alone cannot shift the EWF even with a heat cycle same as the HPOA indicates the oxygen passivation is due to the oxygen diffused through a metal pad, a gate contact and a metal electrode as schematically shown in Fig.13.

CONCLUSION

A novel high-pressure oxygen anneal (HPOA) and high pressure hydrogen anneal (HPHA) processes were applied to MOSFETs with metal electrode/high-k dielectric stack. It has been found that the primary diffusion path of oxygen is through metal gate via gate contact and the diffusion path of hydrogen is primarily through CSEL and spacer nitride. Thus, it is important to properly optimize the gate stack and surrounding dielectric materials to optimize the devices using high

pressure anneal processes. We have shown that the high pressure anneal approach provides a new way to enhance the MOSFETs performance with much lower heat cycle than the conventional FGA, especially for device with metal/high-k stack, providing another means to achieve low temperature process for future scaled devices.

Acknowledgements

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- ISO
- Well
- Gate Stack(3nm ALD HfO2/TiN)
- LDD I/I & S/W
- S/D I/I & Activation
- CESL Nitride

	PECVD	RTCVD
50nm	Control	Control
	Tensile	
	Compress	
100nm	Control	Control

- ILD ~ M1
- HPHA

(a)

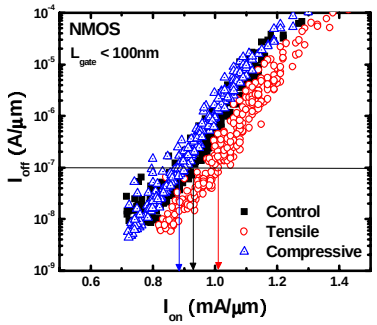


Fig. 2. Comparison of I_{on}-I_{off} performance for nMOS with different stress elements (reference, tensile, compressive).

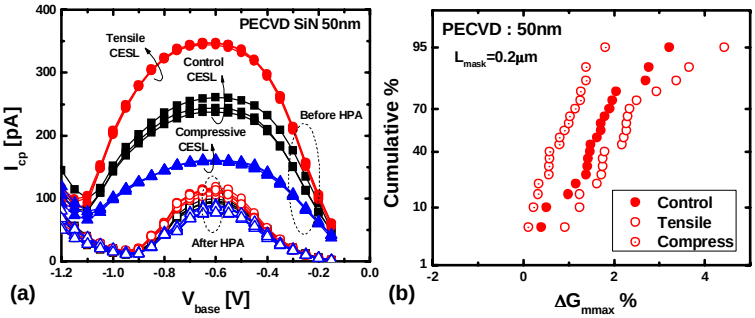


Fig. 3. After HPHA, the interface states were significantly reduced for the all CESL structures. Due to its excess hydrogen, the compressive CESL exhibited the lowest ΔI_{cp}, which resulted in less of a G_{mmax} improvement (b).

- Gate Stack
- w or w/o S/D Anneal
- FGA and/or Post AP and HPO_2 Anneal

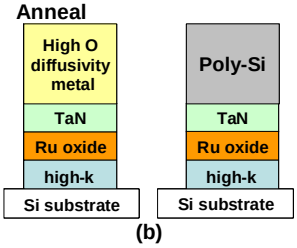


Fig. 1. Process flow and split conditions for (a) HPHA and (b) post-O_2 anneal. The process temperature was <450°C.

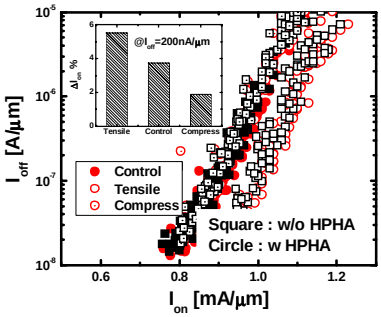


Fig. 4. After HPHA, I_{on} improved 5.4% for the tensile CESL devices due to maximized interface passivation effects.

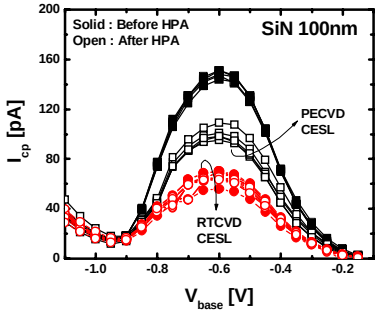


Fig. 5. After HPHA, ΔI_{cp} for the RTCVD CESL samples was negligible.

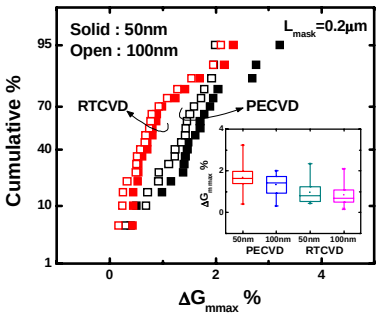


Fig. 6. For both CESL SiN thicknesses, PECVD samples showed more G_{mmax} improvement.

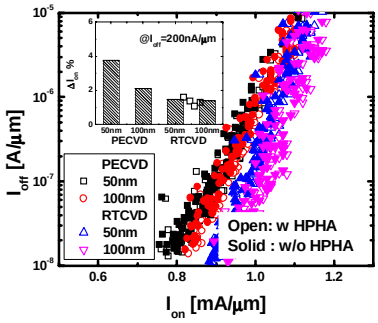


Fig. 7. Less I_{on} improvement was observed for the RTCVD devices due to less hydrogen passivation.

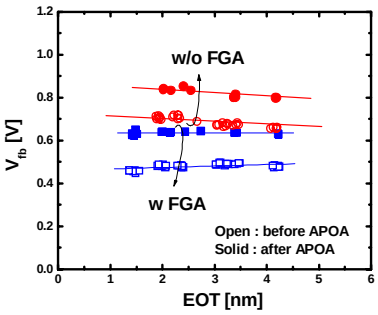


Fig. 8. After APOA, the EWF boost was still observed with and without FGA, and ΔV_{fb} was about 200mV.

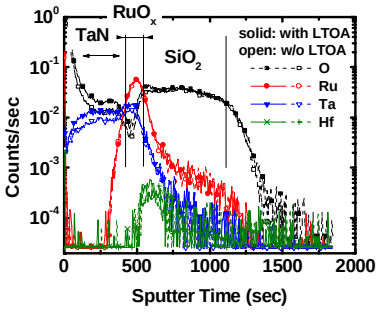


Fig. 9. In the metal gate and capping layer, oxygen concentration was increased after APOA[2].

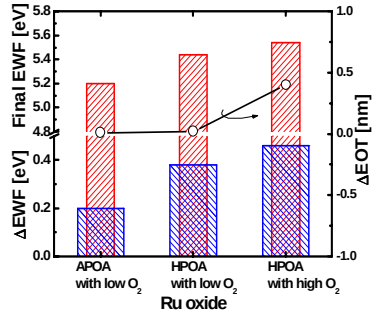
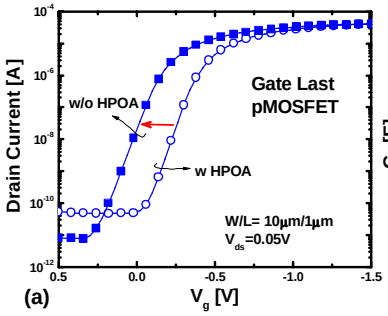


Fig. 10. Comparison of HPOA with low oxygen flow with APOA and high oxygen flow. A 0.4nm EOT change was observed under the high O_2 condition.



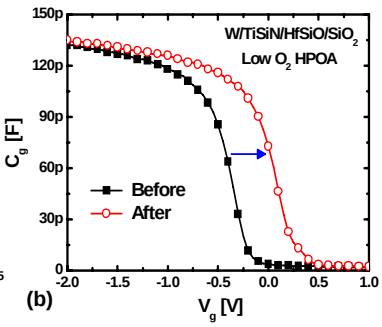


Fig. 11. (a) Transistor I_dV_g characteristics for the gate-last pMOSFET. The V_{th} shift was about 500mV after HPOA. (b) For the gate-first structure, the W-capped structure showed a V_{fb} shift of 500mV.

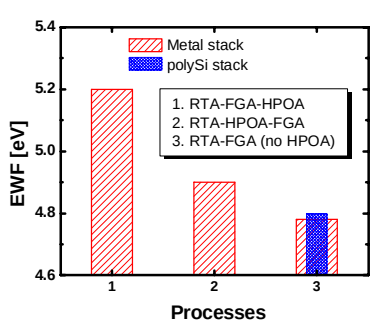


Fig. 12. No EWF change for the poly-Si capped structures, indicating that the poly-Si acted as an oxygen diffusion barrier or contained low initial residual oxygen.

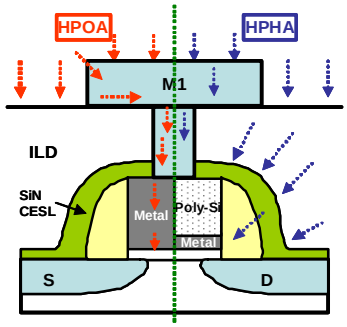


Fig. 13. Schematic of the hydrogen & oxygen diffusion during high pressure anneal. (1) HPOA through the metal gate and (2) HPHA through the ILD and CESL.