Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 24-25

A-2-4

V_t Variation Suppressed Al_2O_3-Capped HfO_2 Gate Dielectrics for Low V_t pMISFETs with High-k/Metal Gate Stacks

T. Morooka, T. Matsuki, N. Mise, S. Kamiyama, T. Nabatame, T. Eimori, Y. Nara, and Y. Ohji

Semiconductor Leading Edge Technologies, Inc., 16-1 Onogawa, Tsukuba, Ibaraki, 305-8569, Japan
Phone : +81-29-849-1299, Fax : +81-29-849-1186, E-mail : morooka.tetsu@selete.co.jp

Abstract

We have systematically studied the effect of post deposition annealing (PDA) for Al_2O_3-capped HfO_2 on flatband voltage (V_{fb}) shift and V_t variation, and found that capped-dielectric process integration has a risk for additional V_t variation. However, we have found that higher temperature PDA process not only brings higher V_{fb} shift but also suppresses this V_t variation. High temperature PDA also has a risk for EOT increase, but process combination of low temperature PDA before Al_2O_3 deposition and high temperature PDA after Al_2O_3 deposition can suppress EOT increase without capping-induced V_t variation.

Introduction

Metal gate/dual high-k CMISFETs have much attention because it is difficult to achieve low V_t CMISFET by common high-k dielectrics [1-2]. Al_2O_3 is a candidate dielectric for pMISFET [3] and existence of Al_2O_3 at the high-k/interfacial layer (IFL) interface plays an essential role in V_{fb} shift [4]. Among many approaches to V_t control, we have proposed single metal/dual high-k (SMDH) CMISFETs in order to simultaneously control V_t and the gate profile (CD, taper, LWR, etc) [5]. However taking account of dual high-k CMISFETs process, not bottom Al_2O_3 deposition under Hf-based high-k dielectric but cap Al_2O_3 deposition on Hf-based high-k dielectric with subsequent Al_2O_3 diffusion to high-k/IFL interface is desirable. In case of this process, removal of high-k dielectrics from IFL is not necessary, so it keeps initial high-k/IFL surface and is integration-friendly. For Al_2O_3 capped high-k dielectrics, thermal annealing condition for Al_2O_3 diffusion to high-k/IFL interface is very important.

In this paper, we have developed the suitable annealing process of Al_2O_3-capped HfO_2 from the view point of V_{fb} positive shift for pMISFET's V_t lowering, reduction of V_t variation and less EOT increase.

Experimental

The process flow is shown in Fig. 1. HfO_2 is deposited as base high-k dielectric, and Al_2O_3 is deposited as V_t controlling high-k dielectric. HfO_2 and Al_2O_3 are deposited by ALD (Atomic Layer Deposition). PDA1, which is post HfO_2 deposition annealing, and PDA2, which is post Al_2O_3 deposition annealing, are applied several at temperatures for 5seconds. After that, TiN and W are deposited by PVD as workfunction tuning metal and low resistive metal, respectively. After gate electrodes are formed by dry etching, extension and source/drain region are formed by ion implant and spike RTA at 1000ºC. EOT and V_{fb} are extracted by "MIRAI-ACCEPT" [6].

Results and Discussion

Fig. 2 shows the CV curves of HfO_2 and Al_2O_3/HfO_2 with several PDA conditions and Fig. 3 shows those V_{fb}-EOT relations. The V_{fb} of Al_2O_3-capped HfO_2 without PDA2 dose not shift from that of HfO_2 and only EOT increases. It suggests that spike RTA (1000ºC) at source/drain activation step is not enough for diffusing Al_2O_3 to high-k/IFL interface. Sequential PDA after Al_2O_3 deposition is needed for V_{fb} positive shift and the shift depends on PDA temperature. The V_{fb} shift is largest at 1050ºC-PDA2 and the value reaches to almost 0.2V.

To investigate the difference between the samples of 850ºC-PDA2 and 1050ºC-PDA2, Al profile is evaluated by 3D atom probe field ion microscopy [7](Fig. 4). The Al concentration profile is most different at HfO_2/IFL interface, and Al segregates at a bottom of HfO2 further more after 1050ºC-PDA2 than after 850ºC PDA2.

Fig. 5 shows the 2D mapping of Al concentration at HfO_2/IFL interface observed by 3D atom probe field ion microscopy. The Al concentrations are fluctuated in the similar manner for both 850ºC- and 1050ºC-PDA2 samples, but higher concentration spots are comparatively infrequent for 850ºC-PDA2. This random fluctuation behavior of Al is considered to have a risk of additional V_t variation on random fluctuation of channel impurity atoms. Fig. 6 shows that $\sigma\Delta V_t$ of pMISFETs with and without Al_2O_3 depends on PDA2 temperatures. $\sigma\Delta V_t$ is the standard deviation of the random offset of the transistor pair, and usually described as following equation [8],

$$\sigma\Delta V_t = \frac{A_{Vt}}{\sqrt{LW}}$$

where L is channel length and W is channel width. The slope A_{Vt} can be considered as the normalized $\sigma\Delta V_t$. In the case with Al_2O_3, the $\sigma\Delta V_t$ of 950ºC-PDA2 and 850ºC-PDA2 are larger than that of 1050ºC-PDA2. Higher temperature PDA at 1050ºC with Al_2O_3 suppresses the V_t variation down to the same level variation of the original HfO_2 without Al_2O_3.

From the view point of V_{fb} shift and V_t variation, 1050ºC-PDA after Al_2O_3 deposition is necessary. On the other hand, 1050ºC-PDA2 has a problem of EOT increase as shown in Fig. 3. For EOT reduction, we tried process integration combined with PDA1 and PDA2. Fig. 7 shows the EOT-V_{fb} plot of single PDA, in which only PDA2 at 850ºC or 1050ºC is applied, and combination PDA, in which both 850ºC-PDA1 and 1050ºC-PDA2 are applied. The combination PDA suppresses EOT increase while keeping the large V_{fb} shift. Because this EOT reduction supposed to be caused by suppression of IFL growth, mobility degradation is anticipated. Fig. 8 shows the hole mobility of HfO_2 and Al_2O_3/HfO_2 of single PDA and combination PDA. Both mobility of Al_2O_3/HfO_2 are almost same, so combination PDA dose not degrade hole mobility. In addition, compared with the mobility of HfO_2, Al_2O_3 capping process dose not degrade hole mobility seriously. Fig. 9 shows the EOT-A_{Vt} Plot of various PDA conditions and various thickness of HfO_2. V_t variation of all Al_2O_3/HfO_2 stacks with 1050ºC-PDA2 are suppressed to that without Al_2O_3 capping. As a result, using combination PDA, EOT = 1.13 nm, ΔV_{fb} = 0.18 V Al_2O_3/HfO_2 stack is achieved without Al_2O_3 capping-induced V_t variation.

Conclusion

The V_{fb} shift and V_t variation of Al_2O_3-capped HfO_2 depend on PDA temperature after Al_2O_3 deposition, and high temperature PDA such as 1050ºC is necessary. Furthermore, process integration combined with low temperature PDA before Al_2O_3 deposition and high temperature PDA after Al_2O_3 deposition can suppress EOT increase without capping-induced Vt variation.

References

[1] S. C. Song et al., VLSI Symp., p.16, 2006.
[2] S. Kubicek et al., IEDM Tech. Dig., p.49, 2007.
[3] H-S. Jung, et al., VLSI Symp., p.204, 2006.
[4] K. Iwamoto et al., VLSI Symp., p.71, 2007.
[5] N. Mise et al., IEDM Tech. Dig., p.527, 2007
[6] N. Yasuda et al., Ext. Abst. SSDM Tech. Dig., p.250, 2005.
[7] A. Cerezo et al., Rev. Sci. Instrum., 59, p862, 1988.
[8] J. M. Pelgrom et al., IEDM Tech. Dig., p.915, 1998.

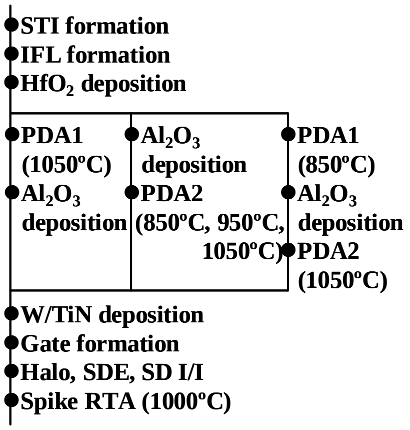

Fig. 1 Process flow of pMISFET with Al_2O_3 capped HfO_2 gate dielectrics. Several PDA conditions are preformed.

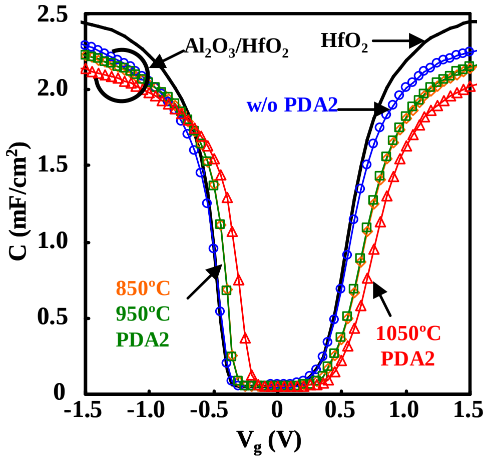

Fig. 2 The CV curves of HfO2 and Al2O3/HfO2 gate dielectrics annealed at several temperatures. Large V_{fb} shift is observed after 1050°C PDA and the V_{fb} without PDA sample is not shifted.

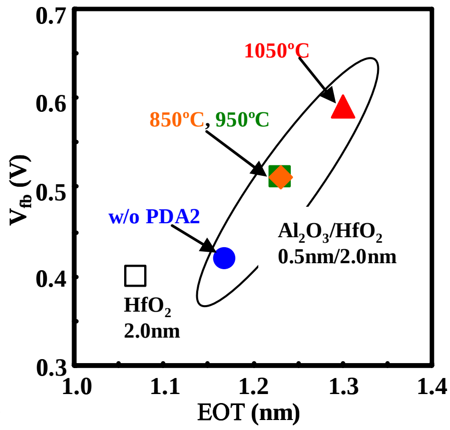

Fig.3 EOT-V_{fb} plot of Al_2O_3/HfO_2 gate dielectrics annealed at several temperatures compared with HfO_2. The V_{fb} shift of 1050°C PDA is the largest.

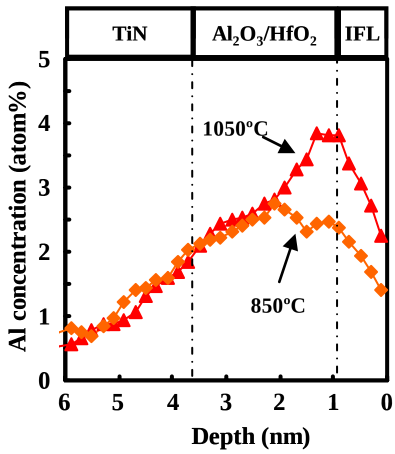

Fig.4 Al profile of 1050°C PDA2 sample and 850°C PDA2 sample evaluated by atom probe field ion microscopy. Large amount of Al atoms are segregated at HfO_2/IFL interface after 1050°C-PDA.

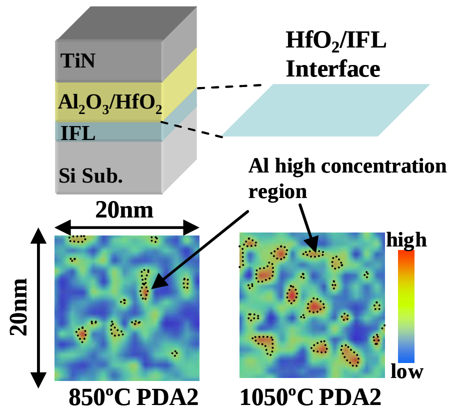

Fig.5 2D-mapping of Al concentration at HfO_2/IFL interface evaluated by atom probe microscopy. High concentration region of 850°C-PDA is infrequent .

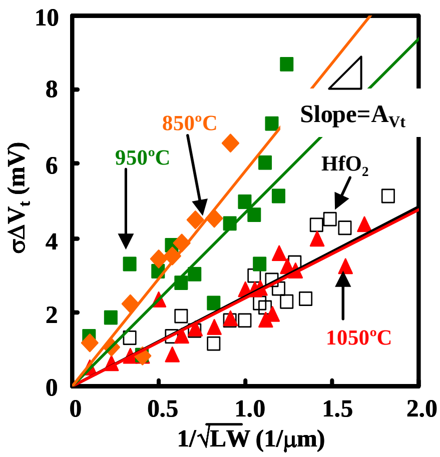

Fig.6 Pelgrom plot of HfO_2 and Al_2O_3/HfO_2 gate dielectrics. Low temperature PDA degrade V_t variation but 1050°C PDA suppress the variation equal to HfO_2 without Al_2O_3.

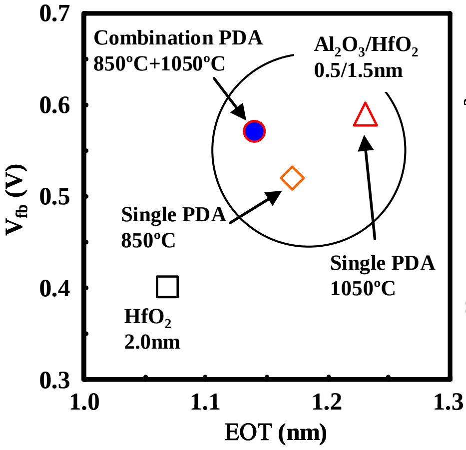

Fig.7 V_{fb}-EOT plot of various PDA conditions. Combination PDA suppresses EOT increase keeping large V_{fb} shift.

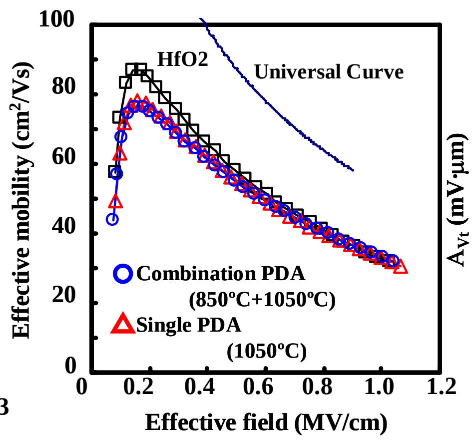

Fig.8 Hole mobility of HfO_2 and Al_2O_3/HfO_2 with single or combination PDA conditions. Significant degradation is not observed with combination PDA.

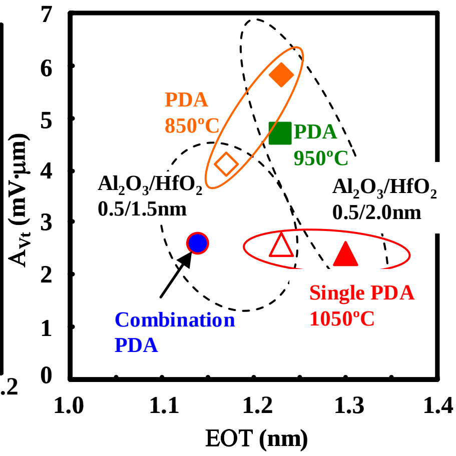

Fig.9 EOT-A_{Vt} Plot of various annealing conditions. A_{Vt} represents the slope of pelgrom plot. Combination PDA suppresses EOT increase and V_t variation.