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Generation of a New Interface-State Associated with Ultra-Thin Gate Dielectrics/Silicon under Electric Stress

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1. Introduction

The reliability of the ultra-thin gate dielectrics is a big issue in Si LSI device-scaling. In such ultra-thin dielectrics, direct-tunneling gate current is observed during operation. It has an impact on estimating the lifetime. As a matter of fact, in the tunneling current region, it is necessary to introduce another lifetime projection models which is different from that successfully applied for thick dielectrics for a long time¹, ². There is a lot of discussion on degradation of the ultra-thin dielectrics³, ⁴, ⁵, but the mechanism remains still unclear. We investigate the interface-state generation that is believed to be a rate-limiting reaction of the degradation serially composed of several elemental reactions. We have found a new interface-state generation in ultra-thin dielectrics after hot electron injection, which has a clear contrast with that in thick one. This new interface state would explain the necessity of the lifetime projection model for ultra-thin dielectrics.

2. Experiments

The samples were fabricated in a standard CMOS process with shallow trench isolation technology. We used N-channel transistors. The transistor channel length / width (L / W) was 5 um / 20 um and oxide thickness (tOX) was 1.6 nm for thin dielectrics, and 1 um / 20 um and 5.5 nm for thick one. The two - level charge pumping (CP)⁵, ⁶ was proposed in Ref. ⁷ and experimentally subtracted the current. To extract the CP current, we modified the method time of the square gate pulse. In thin dielectrics, the direct tunneling current is observed during operation.

3. Results and Discussion

The interface state densities increased against HCI stress time with dielectrics thickness. The characteristics of each condition are different. As shown in Fig. 2(a), a sharp peak grew at Ei + 0.31 eV with 0.05 eV of the width in the thin dielectrics of tOX = 1.6 nm. In the thick one of 5.5 nm, two broad peaks around Ei + 0.25 eV and around Ei + 0.27 eV appeared (Fig. 2(b)). It is noted that these broad peaks also exist in distribution of thin dielectrics when enlarging the vertical scale of Fig. 2(a). We consider these two broad peaks come from so-called structures Pb0 and Pb1, which are common states at SiO2 / Si interface, because their distribution centers are reported respectively to be Ei - 0.25 eV and Ei + 0.30 eV for Pb0, Ei - 0.1 eV and Ei + 0.25 eV for Pb1⁸.

We investigated the origin of the new peak which was found only in thin dielectrics. Because the peak center is very close to the one peak due to Pb0, we first needed to check if this new peak came from the Pb0. We compared mutually the increases of the three peaks such as the new peak and the broad peaks. We used ΔDIT at Ei + 0.31 eV, Ei - 0.25 eV, and Ei + 0.20 eV as the peak intensities. Among these three ΔDIT, one at Ei + 0.20 eV was carefully chosen to avoid the affection from the neighbor. The peak at Ei + 0.31 eV is large enough to neglect the contribution from the broad peak. Such situations are illustrated in Fig. 3. Assuming that the intensity is proportional to the amount of corresponding structure, which is good when the density curve is described by a Lorenzian, these ΔDIT values are able to be discussed on the correlation of the three peaks. Figure 4 shows the correlation of ΔDIT at Ei + 0.31 eV and Ei + 0.20 eV with that at Ei - 0.25 eV. It is obvious that the plots are separated into two. Group A is composed of the ΔDIT at Ei + 0.31 eV, that is the new peak. On the other hand, group B is composed of the broad peaks. The clear separation means that the original structure giving the sharp new peak is different from that of the broad peaks. We thus ruled out the possibility that the new peak was due to common structure for Pb0.

It should also be noted that the plots belonging to group B are well expressed by a straight line in the log-log plot, even though these plots are from both ultra-thin and thick dielectrics. We confirmed that the line included the origin in the liner plot. Their first order relationship means that the two broad peaks are originated from a structure, Pb0, which is consistent with our early assignment solely on a basis of
the location of the distribution peaks.

The atomic-scale structure corresponding to the new sharp peak is unclear so far. The sharpness of 0.05 eV could help determine the structure.

4. Conclusion

We have found a new interface state at $E_i + 0.31$ eV with 0.05 eV of the width in ultra-thin gate-dielectrics / silicon after hot electron injection. This peak is not originated from the common structures giving $P_{b0}$ and $P_{b1}$. The structure giving the new state could lead to another pathway during the degradation, resulting the change of the lifetime projection model for thin dielectrics from well published model for thick dielectrics.

References