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1-nm Spatial Resolution in Carrier Mapping of Ultra-Shallow Junctions by Scanning Spreading Resistance Microscopy

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1. Introduction

High-resolution mapping of carrier distributions in ultra-shallow junctions is required for achieving high performance of CMOSFETs. The lateral/depth spatial resolution for 2D/3D dopant profiles determined by the ITRS is 2.5 nm for 2008 [1], which will become more severe. Scanning spreading resistance microscopy (SSRM) has been shown to be a promising candidate for practical 2D carrier profiling, for the reasons of high spatial resolution and wide dynamic range [2,3], whereas, very little has been reported on the spatial resolution for pn-junction delineation of carriers in silicon devices, despite its technological importance.

When evaluating the spatial resolution of SSRM measurement, the estimated effective probe radius is a determinative factor, which is able to be extracted from the accuracy of the measured pn-junction depth (X_j).

In this report, we carry out both measurements and 3D device simulation of SSRM for ultra-shallow source/drain extension (SDE) junctions of CMOSFETs. The effective probe radius dependence of the extracted X_j of the SDE junction is investigated by simulation. The experimental effective probe radius is estimated by comparing with simulation results, and therefore the spatial resolution is estimated. As an application, the difference of 2D-carrier profiles between pMOSFETs on (100) silicon and (110) direct silicon bonded (DSB) silicon [4] is observed for the first time and there are several new findings.

2. Experimental

SSRM was carried out in a vacuum ($<1 \times 10^{-5}$ Torr) [2]. PMOSFETs were used for measurements. The depth profile of SSRM resistance on the SDE junction is shown in Fig. 1. The corresponding SSRM image is shown in the insert of Fig. 1, where the extracted X_j from the resistance peak is around 11 nm.

To confirm the accuracy of X_j for SSRM measurement, device simulation was carried out on the pMOSFET by an in-house 3D device simulator DIAMOND. Figure 2 shows the setup of the SSRM simulation of a pMOSFET. An SSRM probe with a radius a was scanned across the SDE-halo junction. The parameters were set the same as the experimental ones with a bias of 50 mV and a back electrode with a distance of 5 μm . SIMS results of boron (B) and arsenic (As) dopants were used to calculate the carrier profiles. Majority-carrier profiles were calculated under thermal equilibrium condition. 3D-SSRM simulation was carried out with the two-carrier drift-diffusion model (DDM) [5].

3. Results and Discussions

Simulation results assuming $a = 0.5$ nm are shown in Fig. 3. In Fig. 3, based on the B and As profiles, the net-dopant profiles ($|N_B - N_{As}|$), the majority-carrier concentration profiles, and the carrier profiles derived from SSRM simulation

are shown. It is shown in Fig. 3 that the majority-carrier profile differs from the net-dopant profiles owing to the Debye length limitation, and the simulated SSRM-carrier profiles correspond to and agree well with the carrier profiles other than the dopant profiles. To determine the electrical X_j , the conductivity profile is calculated from the SSRM simulation as shown in Fig. 4, where the extracted X_j from the most resistive point of the majority carriers is around 11 nm. Next, we investigated the probe radius dependence of X_j by changing the probe radius from 0.5 nm to 2 nm, 4 nm, 6 nm, 8 nm, and 10 nm. The results are shown in the insert of Fig. 4. It is found that the extracted X_j increases with increasing probe radius, which deviates from the real electrical junction depth. According to the simulation results, to obtain an accurate X_j of 11 nm, a probe radius of 0.5 nm is required. Because the experimental X_j of 11 nm in Fig. 1 agrees well with the simulated SSRM results in Fig. 4 with a 0.5 nm-probe radius, we confirm that the effective probe radius of our measurement is around 0.5 nm, which enables a high spatial resolution of around 1 nm. The extremely high resolution is attributed to an extremely low parasitic resistance of the whole measurement circuit.

The high-spatial-resolution SSRM is applied to compare the 2D-carrier profiles of pMOSFETs on (100) silicon and (110) DSB substrates with varying DSB thickness as shown in Figs. 5(a) to (d), respectively, and the profiles are shown in Fig. 6. From Fig. 5, several features are found on (110) pMOSFETs: 1) the P^+/n -well junction depth varies with DSB thickness; 2) the lateral diffusion of carriers is observed along the DSB interface; 3) the carriers pile up on the DSB interface. Furthermore, the lateral diffusion shows DSB thickness dependence and becomes more pronounced with shallower DSB thickness in the SDE region. This feature may account for the Cov degradation of shallow DSBs [4]. From Fig. 6, the carrier piling up on DSB interface may account for the increased junction leakage with a DSB thickness coincident with the junction depth [4].

4. Conclusions

We confirmed the 1-nm spatial resolution of SSRM in carrier profiling by comparing with 3D device simulation. The simulation results show that the accuracy of ultra-shallow-junction delineation depends on the effective radius of the probe. The precisely measured junction depth corresponds to an effective probe radius of 0.5 nm. Applications to the comparison of pMOSFETs on (100) and (110) silicon clarified the 2D-carrier behaviors on DSB substrates.

References

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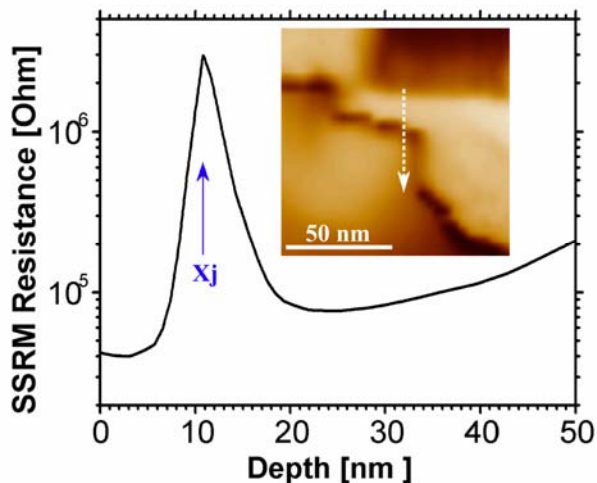


Fig. 1. The depth profile of SSRM resistance on the SDE junction of a p-type MOSFET. The corresponding SSRM image is shown in the inset of Fig. 1. The extracted X_j is around 11 nm.

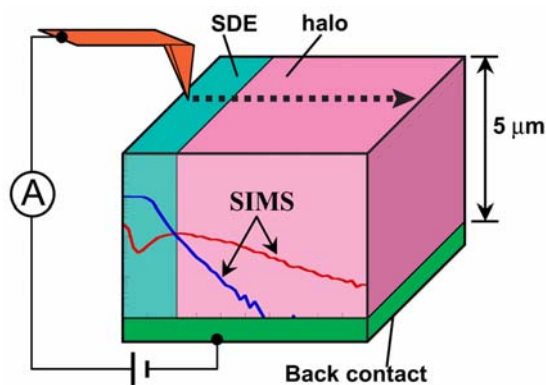


Fig. 2. The setup of the 3D simulation of SSRM. The effective radius of contact area between the probe and the sample is assumed to be a . The SIMS profiles of B and As were input for calculations.

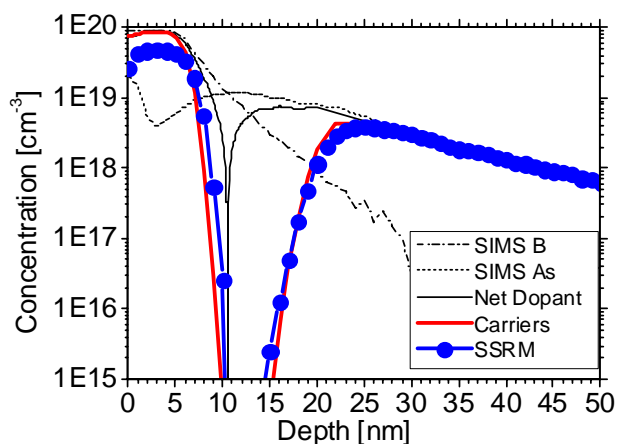


Fig. 3. The simulation results of SSRM assuming $a = 0.5$ nm. The net-dopant profile, the majority-carrier concentration profiles, and the carrier profiles extracted from 3D SSRM simulation are shown, based on the SIMS profiles of B and As

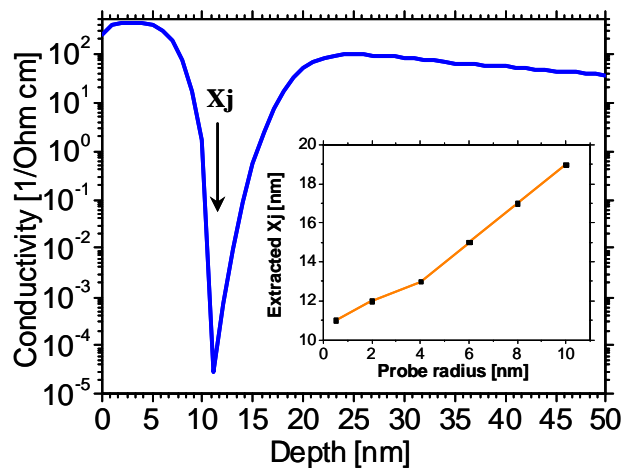


Fig. 4. The conductivity profile calculated from the SSRM simulation ($a=0.5$ nm). The effective radius dependence of the electrical X_j is shown in the inset.

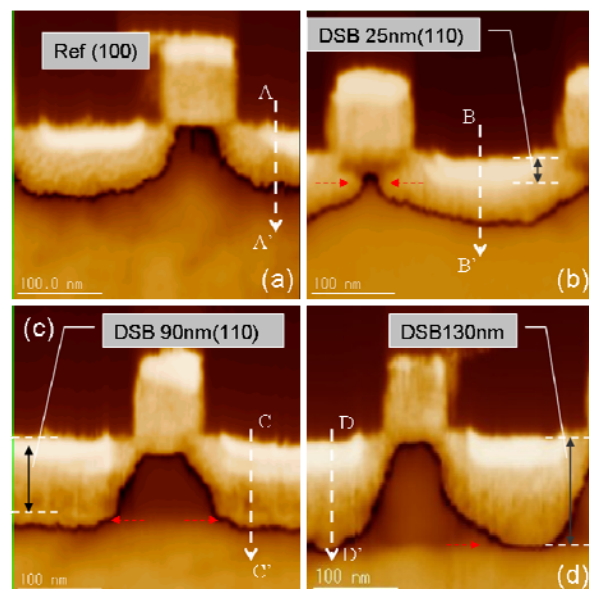


Fig. 5. Comparison of carrier mapping for (a) (100); (b)-(d) DSB (110) silicon with DSB thickness of 25 nm, 90 nm, and 130 nm, respectively.

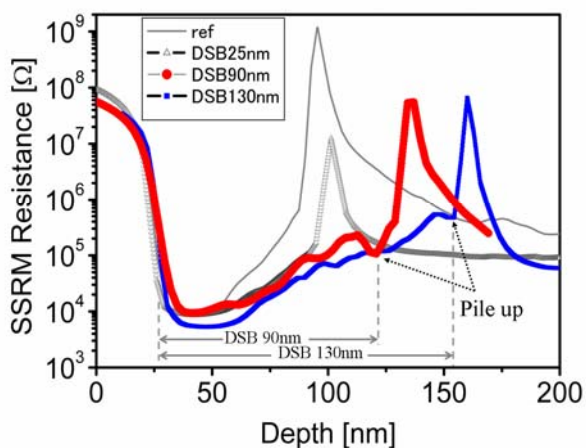


Fig. 6. SSRM-resistance profiles along AA' to DD' in Fig. 5 (a)-(d).