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Carrier density mapping of small n-MOSFET devices by vacuum-gap modulation scanning tunneling spectroscopy

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1. Introduction

As the scaling down of Si MOSFETs has reached the device size below 65 nm, measurements of the device properties at an atomic scale has become crucial to optimize performance of ultra-small devices. Scanning tunneling microscopy (STM) is a promising technique as it has shown the ability to visualize individual impurity atoms and to determine variation of the surface potential on passivated Si surfaces and device cross-sections. [1, 2] We have already shown that spatial variation of the surface potential due to negative acceptor charges beneath the Si surface were obtained in local work function (LWF) maps on oxygen-passivated surfaces of Si(111) and (110) by vacuum-gap modulation (VGM) STM spectroscopy. [3]

In this paper we investigate origin of the LWF variation on cross sections of small n-MOSFET devices with gate lengths in a range of 12 - 150 nm by the VGM-STM spectroscopy. We show that the LWF map reflects carrier concentration rather than built-in potential distribution. In particular, lack of carriers in the depletion region results in a distinctive minimum in LWF maps. We made use of the feature to determine the electrical channel length with a nanometer resolution.

2. Results

VGM spectroscopy technique

Essential difference between STM junctions on metal and passivated Si surfaces is illustrated in Fig.1. For metallic surfaces, the applied voltage V_0 is held by the vacuum gap (V_{gap}) but for Si samples it is shared by the band bending region (V_{bb}) beneath the surface modifying the tunneling barrier.[4] The voltage drop in the vacuum gap is determined by strength of electric field F_{gap} at the Si surface and, in turn, is a function of density of mobile carriers P_S and static charges N beneath the surface. Consequently, variation of the tunneling current dI in response to small modulation of the gap width dZ can be expressed as

$$\frac{dI}{I_0} \propto F_{gap}\left[P_s + N\right] \cdot dZ \,, \qquad (1)$$

where the mean tunneling current I_0 is held constant (i.e. the mean gap barrier is constant). Therefore, the measured LWF maps represent charge distribution beneath the Si surface.

The STM probe-sample gap was modulated at 17 kHz with an amplitude dZ of 20 pm while the mean tunneling current I_0 was maintained constant. [3] Current response dI was measured with a lock-in amplifier at each point in the topographical image, and the LWF value was calculated from measured *(dI/dZ)* signal as [4]

$$LWF = 0.95 \cdot \left(\frac{dI}{I_0 \cdot dZ} \right)^2 \cdot \qquad (2)$$

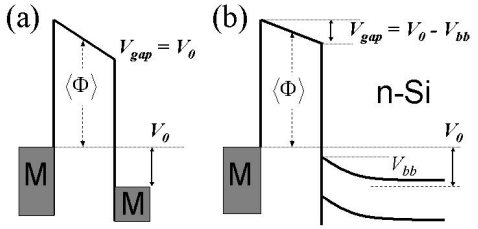

Fig. 1 Energy diagrams of STM junctions at metal (a) and semiconductor (b) samples under a bias voltage V_0.

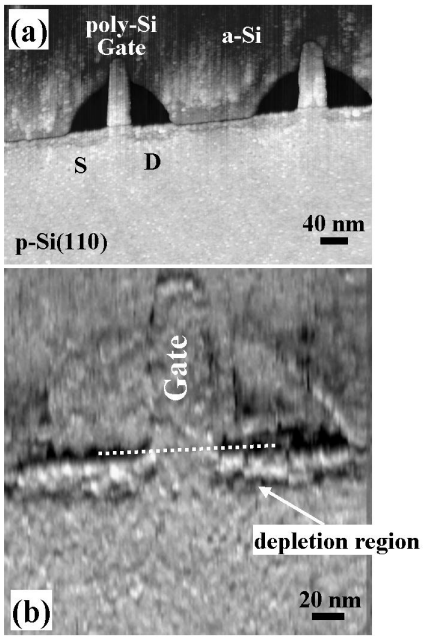

Fig. 2 (a) STM topograph of two *n*-MOSFET devices. (b) LWF map of one device with a gate length of 35 nm obtained at a bias voltage of 3.4 V and a tunneling current of 130 pA. The dotted line indicates the gate oxide position.

Carrier density mapping

Samples of *n*-MOSFET devices were prepared with gate lengths in the range of 12 – 150 nm according to the normal fabrication process described in Ref. [1]. Cross sections of the devices were prepared by ultra-fine polishing to expose (110) surfaces. Surfaces were passivated by ultra-thin oxide layers grown at ~600°C under an O_2 pressure

of $3x10^{-3}$ Pa following etch-cleaning in HF:HCl (1:19). [3] The measurements were done in an ultra high vacuum (~4×10^{-9} Pa) at room temperature.

Figure 2(a) shows a typical STM topograph of the oxidized cross sectional surface. Side-wall insulators besides the gates appeared as dips produced during surface etch-cleaning. The LWF map of a device with L_G = 35 nm in Fig. 2(b) shows that the channel region beneath the gate electrode separates two narrow bright (i.e. high carrier density) areas – the drain (D) and source (S) extensions. Narrow dark regions (a low LWF) adjacent to the drain/ source extensions correspond to depletion regions at *p-n* junctions formed between the *n*-type extensions and the *p*-type channel. Roughness seen in the channel region is due to individual subsurface charges such as charged dopant atoms and defects.

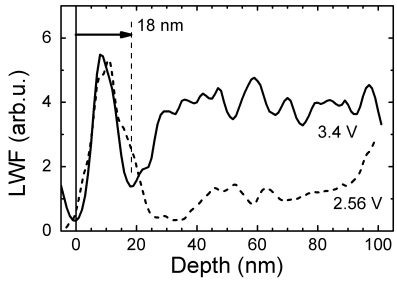

Fig. 3 Average depth profiles of the LWF across the drain extension (the peak at ~10 nm) away from the gate. The gate oxide position is at zero.

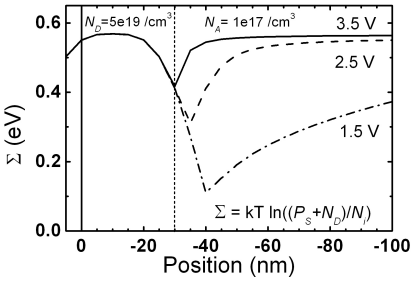

Fig. 4 Simulated profiles of the surface potential across *p-n* junction at three STM probe bias voltages. The dotted line indicates an abrupt junction position at 30 nm where $N_D = N_A$.

Depth profiles in Fig.3 show large LWF values in the drain extension. A distinctive minimum was at 18 nm below the gate oxide at the bias voltage of 3.4 V, while it was at ~30 nm at 2.56 V.

To assess origin of the LWF minimum seen in Fig.3, we calculated charge density under the STM probe by solving the Poisson equation at different probe-sample bias voltage. Profiles in Fig. 4 represent variation of the charge density across an abrupt *p-n* junction, and reproduce the behavior observed in Fig. 3. The result suggests that the observed LWF minimum appeared due to lack of carriers at a position of the electrical *p-n* junction under the bias voltage.

Measurements of channel lengths

Positions of electrical *p-n* junctions between the channel and the extensions were obtained from lateral profiles as illustrated in Fig. 5 for two devices with L_G = 60 nm and 31 nm. To improve the resolution we took advantage of narrowing of the depletion region at 3.4 V. The L_G was determined from STM topographs. The measurement results are summarized in Fig. 6. An overlap between the gate and the extensions of $\Delta L = 8 \pm 1$ nm was obtained for short-gate devices.

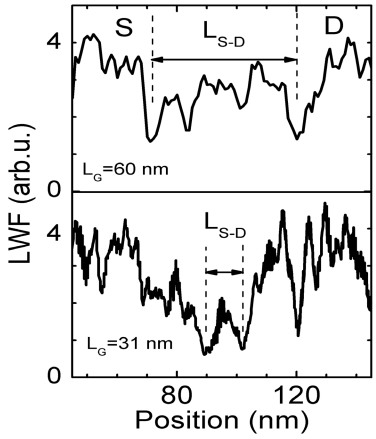

Fig. 5 Line profiles of the LWF across channel regions at a depth of 12 nm beneath the gate oxide for two devices at the bias voltage of 3.4 V.

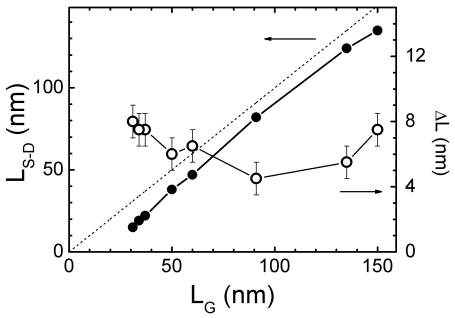

Fig. 6 The channel length $L_{S\text{-}D}$ (solid circles) and the gate/ extension overlap (open circles) *vs.* gate length L_G.

3. Conclusions

We assessed the ability of the VGM spectroscopy for high resolution mapping of charge distribution in small Si devices. The distinctive bias-dependent feature in the LWF map revealed the electrical p-n junction and was utilized to determine the channel length with a nanometer resolution.

Acknowledgements

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References

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