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Trap Generation in $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3$ High- κ Gate Stack by Nanoscale Electrical StressY. C. Ong¹, D. S. Ang¹, S. J. O'Shea², K. L. Pey¹, C. H. Tung³, T. Kawanago⁴, K. Kakushima⁴, H. Iwai⁴¹School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (E-Mail: N040136@ntu.edu.sg)²Institute of Materials Research and Engineering, 3, Research Link, Singapore 117602³Institute of Microelectronics, 11, Science Park Road, Singapore Science Park II, Singapore 117685⁴Frontier Collaborative Research Center, Tokyo Institute of Technology, 4259 Nagatsuta, Midori-ku, Yokohama, 226-8502, Japan**1. Introduction**

Non-uniformity is an inherent problem in most high- κ gate dielectrics [1]. As a result, the conventional MOS capacitor technique for reliability study might reflect the extrinsic phenomenon instead of the intrinsic degradation mechanism of the dielectrics. In Scanning Tunneling Microscopy (STM), with the capability of imaging the property of the high- κ and interfacial layer (IL) independently at high spatial resolution [2], fresh areas without pre-existing defect can be identified subsequently. Electrical stressing within this area is expected to reveal the intrinsic degradation mechanism in the bi-layer dielectric gate stack. Using this STM local stressing method, we observe (1) a substantially higher trap generation rate in the high- κ layer; and (2) the locations of worst-case trap generation (giving rise to localized high leakage current) in the high- κ layer generally do not correspond to those in the IL. The "mismatch" in the locations of trap generation in the high- κ and IL may give additional reliability margin to the high- κ gate stack.

2. Experimental

The bi-layer gate stack, consisting of 3 nm Sc_2O_3 (top) and 4 nm La_2O_3 on a n-Si substrate, was prepared by electron-beam vapor deposition in ultra-high vacuum (UHV) with HF-last Si surface preparation. Post-deposition anneal was done in nitrogen at 500°C. The IL is ~1 nm thick. A UHV STM was used to study the gate stack at nanometer spatial resolution. The biasing voltage V_s was applied to the substrate. STM images were obtained at a biasing condition of -4 V, 20 pA (bias set point). The tunneling current was maintained constant by a feedback circuit. The constant current image (z map) of the high- κ gate stack contains information on both film morphology and electrical properties. To examine the electrical properties of the gate stack separately, CITS was acquired by measuring the current-voltage (IV) at each pixel. Feedback was interrupted after ~20 ms (the time taken for feedback set point to stabilize) and V_s was ramped from -4V to +4V at ~60 mV/ms, while tunneling current was simultaneously recorded. The tunneling current at each pixel can be combined to form a current map of the scanned area at a given voltage for identification of localized high leakage sites in the dielectric stack. Each complete CITS scan of the selected area took ~48 minutes.

3. Results and Discussion

Higher Trap Generation Rate in the High- κ Electronic trap generation can be delineated as a localized high leakage spot (bright shades) in the CITS current map. As already shown [2], due to the polarity dependence of the tunneling current, CITS image corresponding to a positive (or negative) V_s can serve as sensitive monitor for trap generation in the high- κ (or IL) layer. Stress induced trap generation was monitored through the observation of localized high leakage sites in the CITS image. Image contrast was adjusted such that the top 5th percentile of the leakage current distribution, which corresponds to the "leakiest" spots within the scanned area, appear bright.

A 50 nm x 50 nm region initially free of localized high leakage sites (i.e. no pre-existing traps) in both the high- κ and IL was

chosen, as shown by the uniform CITS image in Fig 1 (a, II-IV). The region was then subjected to repeated CITS scans. Bright shades, which correspond to localized high leakage sites, are observed after subsequent scans, signifying electronic trap generation in the dielectric stack. For the CITS image at -2.3V, bright shades, due to trap generation in the IL are observed only at the 3rd and subsequent scans. On the other hand, at positive V_s (column III & IV), bright spots are observed starting from the 2nd scan [Fig. 1 (b, III & IV)]. The CITS images at positive V_s for the 5th scan [Fig. 1 (c, III & IV)] show bright shades at locations different from those observed at the 2nd scan (Fig. 1(b)). This is because bright shades in Fig. 1(b) have been suppressed due to the generation of new leakage spots with higher leakage current at other locations upon the 5th scan. Fig. 2 and 3 depict tunneling current distributions at -2.3V and +4V for all the 5 scans. For the former, the top 5th percentile of the leakage current distribution remains relatively constant at ~1.5 pA for all scans. For the +4V, however, the top 5th percentile is increased (from an initially negligibly low level; i.e. < 0.1 pA) significantly to 12 pA, accompanied by an increase in scatter, for the 3rd and subsequent scans. Fig. 4 shows that the averaged tunneling spectrum of the 1st scan has negligible current at positive V_s . On the other hand, the averaged IV of the bright shades [Fig. 1(b), (c); III & IV] depicts a significant leakage current in the positive V_s regime. These observations point to an earlier onset of more significant electronic trap generation in the high- κ layer (Fig. 5) as compared to IL.

Mapping the Location of Trap Generation in the High- κ and IL

Fig. 6 is a superposition of the CITS images obtained under positive and negative V_s , showing that the leakiest spots in the high- κ layer generally do not correspond to those in the IL. Indeed, the averaged IV corresponding to the bright shades in a negative V_s CITS image is substantially lower in the positive V_s , as compared to the IV corresponding to bright shades in a positive V_s CITS image (Fig. 7). These observations imply that the locations of worst-case trap generation are different in the 2 layers. Moreover, it seems that existing traps in the IL would "suppress" trap generation in the high- κ at the same locations [3]. As traps in the high- κ must align to those in the IL for breakdown to occur (under the framework of the percolation model [4]), the general mismatch in the locations of worst-case trap generation in the 2 layers may give additional reliability margin to the high- κ gate stack.

4. Summary

This STM study presents physical evidence for (1) a substantially higher trap generation rate in the high- κ layer; and (2) the locations of worst-case trap generation in the high- κ layer generally do not correspond to those in the IL.

References

- [1] Miranda *et al.*, J. Non-Crystalline Solids 352, 92, 2006;
- [2] Ong *et al.*, Appl. Phys. Lett. 92, 022904, 2008;
- [3] Zhao *et al.*, Microelectron. Eng. 80, 366, 2005;
- [4] Nicollian *et al.*, in IEDM Tech. Dig. 2006, pp. 1.

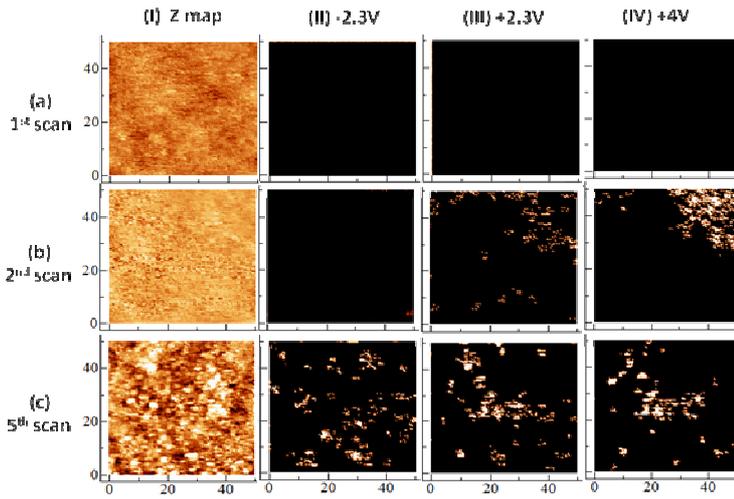


Fig. 1 Rows a, b and c show the CITS corresponding to the 1st, 2nd and 5th consecutive scan, respectively. Column I, II, III and IV show the topography image, the CITS image at $V_s = -2.3$ V, $+2.3$ V and $+4$ V, respectively. The contrast of the CITS image is adjusted such that locations exhibiting tunnelling leakage within the top 5th percentile of the current distribution are shown as bright shades. This is defined as “cut-off current” and its value varies depending on the degree of degradation (i.e. trap generation). This procedure is done to locate the leakiest path within the scanned area. CITS images with a relatively uniform tunnelling current distribution appear entirely dark as a cut-off current cannot be effectively located. The selected area is initially free of leakage path (1st scan). Leakage path is first generated in the high- κ layer (2nd CITS, row b) then at the IL in the subsequent scans. Bright spots at the 5th scan (row c, III and IV) occur at different location compared to those of the 2nd scan (row b, III and IV). This is because new localized leakage paths of higher current are generated at different locations at subsequent scans, thus “suppressing” the appearance of old leakage paths which do not degrade further.

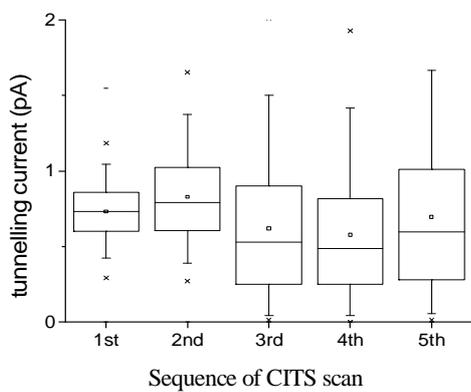


Fig. 2 Tunnelling current distributions of 50×50 nm scanned area at $V_s = -2.3$ V (This V_s probes electronic trap generation in the IL). The upper whisker of the box plot corresponds to the top 5th percentile used to generate the CITS images in Fig. 1, column II.

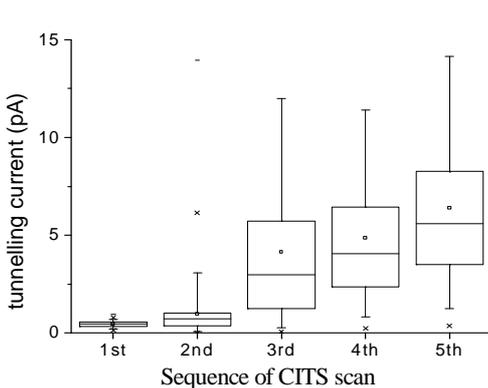


Fig. 3 Tunnelling current distributions of 50×50 nm² scanned area at $V_s = +4$ V (This V_s probes electronic trap generation in the high- κ layer). The upper whisker of the box plot corresponds to the top 5th percentile used to generate the CITS images in Fig. 1, column IV.

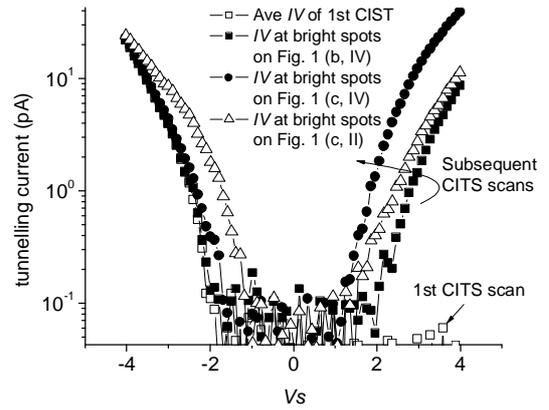


Fig. 4 Comparison of IV from various CITS scans. The IV of the 1st scan is the average of all pixels in the scanned area. For subsequent scans, the IV of the bright shades in the CITS images shown in Fig. 1 (column II to IV) are plotted.

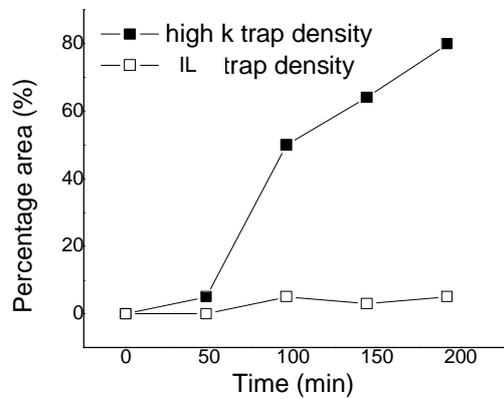


Fig. 5 Percentage of the scanned area having stress induced leakage current exceeding a chosen threshold current. The selected criterion corresponds to the top 5th percentile of the leakage current distribution of the 2nd CITS. “Time” refers to the period taken to complete one CITS scan. The slope of the curve gives an estimation of the trap generation rate. Trap generation rates for the high- κ and IL layers are estimated to be 11.5 nm²/min and 0.55 nm²/min, respectively.

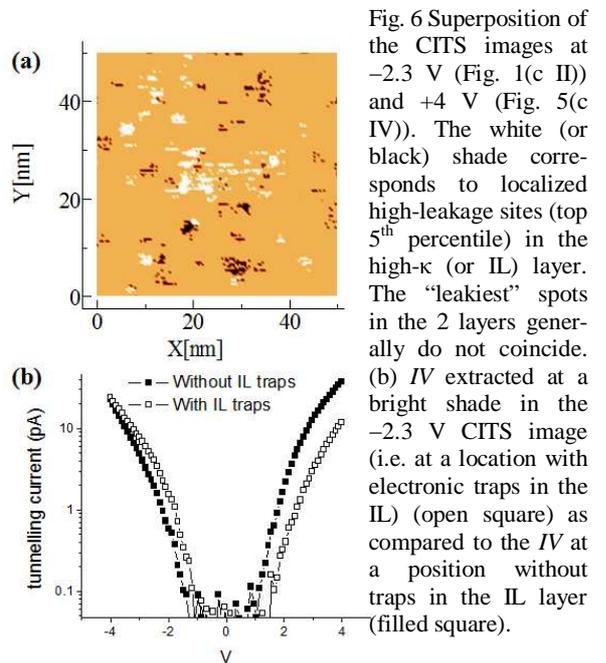


Fig. 6 Superposition of the CITS images at -2.3 V (Fig. 1(c II)) and $+4$ V (Fig. 5(c IV)). The white (or black) shade corresponds to localized high-leakage sites (top 5th percentile) in the high- κ (or IL) layer. The “leakiest” spots in the 2 layers generally do not coincide. (b) IV extracted at a bright shade in the -2.3 V CITS image (i.e. at a location with electronic traps in the IL) (open square) as compared to the IV at a position without traps in the IL layer (filled square).