Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 680-681

A-5-1

Defect profiling and the role of nitrogen in lanthanum oxide-capped high-κ dielectrics for nMOS applications

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Results from an extensive reliability characterisation of Lanthanum oxide-capped HfSiO(N) devices are reported for the first time. It is shown that the effect of nitrogen presence in the high-κ is significant; whereby the ability of lanthanum oxide to interact with the high-κ dielectric is reduced, with detrimental consequences on device reliability. A profile of defects in the gate stack is proposed, inferred from a combination of reliability measurements.

Introduction

The quest to achieve band edge effective workfunction values for sub 32 nm CMOS devices looks unlikely to be resolved solely by choice of electrode on a single high-κ dielectric layer. It is becoming more evident that an additional dielectric layer will be required to tune the threshold voltage/effective workfunction. To date, rare earth capping layers have been reported to effectively reduce the threshold voltage on nMOS devices, where up to 500 mV V_t tuning can be achieved, depending on the La_2O_3 cap/high-κ combination [1-3]. However, to date no extensive reliability characterisation of these capped dielectrics has been reported, in terms of defect profiling in the stack resulting from various analysis techniques. This provides the aim of this work, using gate/dielectric stacks with promising Vt/eWF characteristics.

Experimental

nMOS devices were fabricated with 1.0 nm chemical oxide starting surface. 2.9 nm (unless specified) MOCVD HfSiO was deposited and was subsequently nitrided by a plasma process. 0-1.0 nm ALD La_2O_3 cap layers were deposited, before sputtering TaN electrodes, junction activation annealing at 1030°C, and forming gas annealing.

Results

Using TaN as the gate electrode presents thermodynamically stable (although midgap) material, which when combined with a 1.0 nm La_2O_3 cap, results in V_{fb}/V_t tuning capabilities up to 270 mV (Figure 1). From the inset, it is clear the V_t values reduce with increasing cap layer thickness, and also the $g_{m\ peak}$ values decrease. There is no significant change in the interface state density as evaluated from base level charge pumping (Figure 2), suggesting the transconductance/ mobility reduction is related to a presence of bulk charge. PBTI analysis on the capped and reference sample indicate enhanced electron trapping in the capped film relative to the reference (Figure 3). The 10 year operating voltage (for 30 mV ΔV_t) reduces from 1.33V for the uncapped film to 1.01V for the 1.0nm cap case. The degradation under hot carrier stressing is shown in Figure 4 to be higher for the capped film (where the 10 year lifetime is reached at 1.84V, compared to 1.92 V for the uncapped reference). Hysteresis in I_d-V_g traces indicate increased electron trapping with cap thickness (Figure 5), both at the Si/SiO_2 interface (deduced from the slight transconductance peak degradation during hysteresis measurement [4]) and predominantly deeper in the stack (from threshold voltage shift in Figure 5 [5]). TDDB lifetime of the devices increases with the thickness of the cap layer (Figure 6), from 1.03 V to 1.15 V for the uncapped and 1.0 nm capped films, respectively, which is believed to result from the increased physical thickness of the dielectric layers, as evidenced in the difference in inversion capacitance (Figure 1). To summarise the results of the TaN/1.0 nm La_2O_3/2.9 nm HfSiON stacks, it is shown that a strong V_t reduction is achieved, however this is achieved at a cost to the reliability. As the CET of these films is higher than that targeted, a further study was performed on thinner dielectrics.

Given the negative effects of lanthanum incorporation on reliability, both the high-κ and cap layer thickness were scaled down (to 1.8 nm and 0.7 nm, respectively) in a bid to reduce the thickness of the stacks. An uncapped reference was also examined. No nitridation was performed on the dielectric, which were deposited on n and pMOS samples. The effect of this is a 380 mV V_t reduction with 0.7 nm La_2O_3 layer incorporation, at 1.6 nm CET. The BTI characteristics are presented in Figure 7, where the 10 year lifetime is achieved for reference and capped films at gate overdrive values of 0.79V and 0.92 V, respectively after PBTI stress. Interestingly the lifetime is increased by the presence of the cap. NBTI analysis of the La_2O_3 capped devices demonstrates a reduced lifetime with cap layer. The peak transconductance degradation during NBTI stressing is enhanced for the capped layer (not shown), which indicates an increase in interface state generation [4]. The degradation under hot carrier stressing is shown in Figure 8, where the 10 year lifetime is reached at V_{ds} = 1.92 V with cap, and 1.94 V for the uncapped reference. The current-time traces during substrate (V_g>0, Figure 9) and gate (V_g<0, Figure 10) injection are shown for reference and capped films to help explain these results. From substrate injection, the fast initial transient for the capped film is consistent with electron trapping in the high-κ, as detected in PBTI and I_d-V_g (see below). From gate injection, the initial transient suggests enhanced electron trapping in the SiO_2 interface layer, which could explain the hot carrier degradation for the capped film (Figure 8). TDDB results are presented in Figure 11, and it is seen an increased 10 year operating voltage is obtained with the cap (1.07 V compared to 0.90 V for no cap). The beta values increase from 1.05 for the uncapped film, to 1.49 for the capped (also seen for La_2O_3 capped pMOS devices (not shown)), suggesting a difference in the defect creation mechanism throughout the stack. This is further proof of a significant interaction between the cap layer and the host dielectric. From repeat I_d-V_g sweeps on nMOS and pMOS devices in Figure 12, slight (positive) hysteresis is seen on the nMOS capped layer.

Defect distribution and the role played of nitrogen

There is a significant difference in the reliability characteristics of the two series of gate stacks examined in this work. Adding 1.0 nm La_2O_3 to 2.9 nm HfSiON results in a deterioration of reliability characteristics, whereas adding 0.7 nm La_2O_3 to 1.8 nm HfSiO enhances the reliability. As only the first sample set received a nitridation step, this is believed to result in an increased thermodynamic stability [6], whereby interaction between La_2O_3 and $HfSiON/SiO_2$ is less than that between La_2O_3 and $HfSiO/SiO_2$. This agrees with the cap induced effects observed, notably (1) a higher V_t shift (Figures 12 & 5) and (2) the significant TDDB-beta value increase for the non-nitrided stack (Figures 11 & 6).

Combining these results can lead to a defect profile in the band gap as shown in the inset of Figure 12. Defects are seen at the Si/SiO_2 interface ([A] $E>E_i$ from Δg_m peak during I_d-V_g hysteresis/HCS (with higher density for the non-nitrided film), [B] $E<E_i$ from NBTI), and in the high-κ layer ([C] close to the MG/hi-κ interface; from voltage dependence of PBTI and evolution of I-t traces, and [D] close to the SiO_2/hi-κ, from NBTI). The convergence of PBTI degradation for capped and uncapped films (Figure 7B) with reducing stress conditions suggests the dominant defects in the capped films are at an energy level whereby they will not be accessed during device operation. The defects in the interface layer of the non-nitrided film, accessed during HCS measurements (Figure 8) do not radically shift the lifetime, suggesting a relatively low density, which again is promising from a reliability perspective. Coupled with the V_t-tuning potential of these layers, they provide a promising reliable route for future generation CMOS scaling.

Conclusions

This work provides an extensive reliability characterisation of dielectric stacks for the 32 nm node, which incorporate rare earth (lanthanum) oxide capping layers. It is shown that the effect of nitrogen incorporation is significant on the reliability of lanthanum oxide containing devices. A defect distribution is proposed throughout the gate stack to explain the results observed.

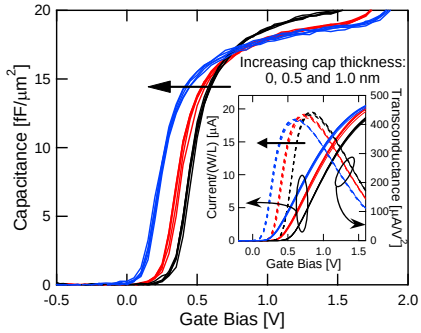

Figure 1. C_{gc}-V for La_2O_3 capped TaN-gated transistors shows V_t and CET reduction with cap insertion. Inset shows the I_d-V_g (negative) shift and peak g_m degradation with cap presence and thickness.

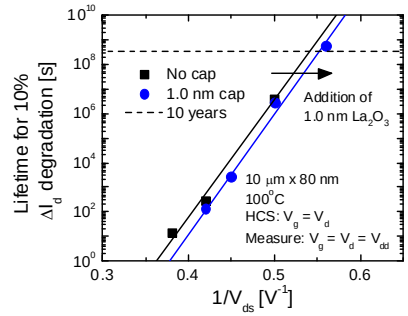

Figure 4. Lifetime extrapolation for degradation due to hot carrier stressing. Similar voltage acceleration of the degradation is detected for both samples, which is enhanced for 1.0 nm cap.

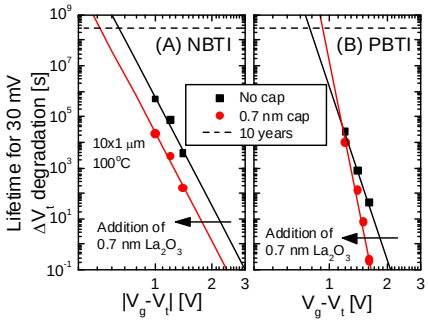

Figure 7. BTI lifetime extrapolation for La_2O_3 capped HfSiON. (A) NBTI lifetime is degraded by the cap, whereas (B) PBTI is enhanced, due to a stronger voltage dependence than the uncapped reference.

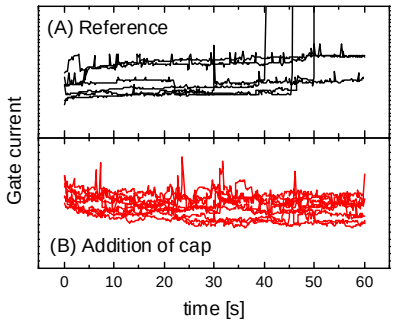

Figure 10. Current-time traces during gate injection (negative gate bias) for (A) reference and (B) La_2O_3 capped films. Note the initial transient for the capped film (for t<15s), consistent with electron trapping in the SiO_2 interface layer, not seen for the uncapped reference case. After the transient, a similar defect creation rate is seen in both cases (as inferred from $\delta I_g/\delta t$).

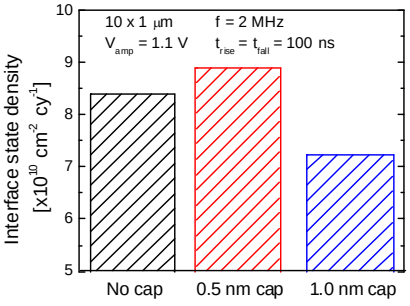

Figure 2. Interface state density as deduced from base level charge pumping as a function of La_2O_3 cap thickness.

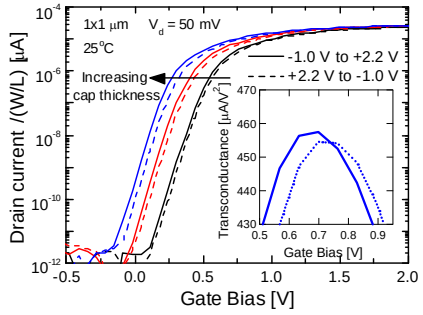

Figure 5. Hysteresis in I_d-V_g characteristics increases with cap thickness. A slight transconductance peak degradation (inset) indicates the V_t shift predominantly results from electron trapping and only partially due to interface state creation.

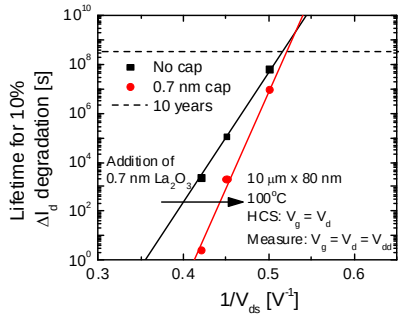

Figure 8. Lifetime extrapolation under hot carrier stressing. 10 year lifetimes achieved at V_{ds} = 1.92 V and 1.94 V for capped and reference films. As for PBTI, a higher voltage dependence is observed for the capped film than the reference.

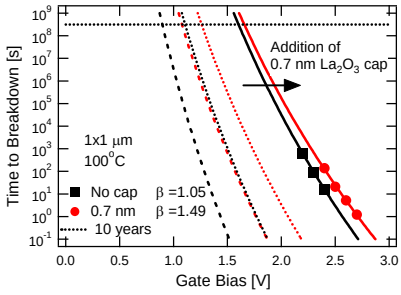

Figure 11: Effect of 0.7 nm La_2O_3 cap on TDDB lifetime, after scaling to 0.1 cm^2 and 0.01% is a significant improvement in 10 year lifetime, and increased beta value.

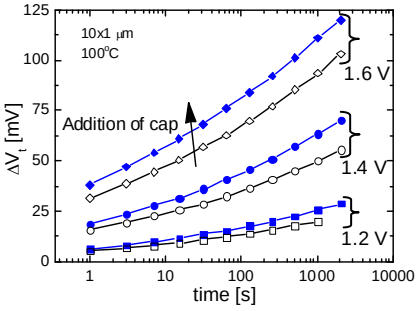

Figure 3. ΔV_t due to PBTI stress for 1.0 nm cap (solid) and non capped reference (open) with TaN gate at a range of V_g-V_t values. Higher electron trapping is detected in the capped film, while no effect is seen on the Si/SiO_2 interface characteristics (not shown).

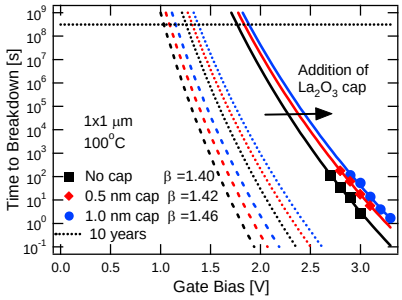

Figure 6. TDDB lifetime, scaled to 0.1 cm^2 and 0.01% indicates an enhancement with cap thickness, and a marginal increase in beta value with cap thickness.

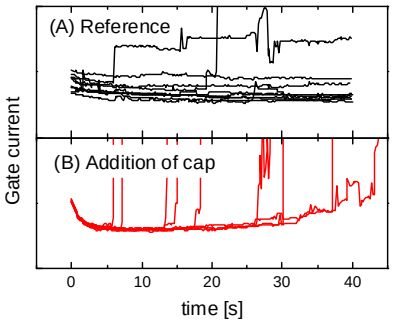

Figure 9. Current time traces during substrate injection (V_g>0) stress for (A) reference and (B) La_2O_3 capped films. Note the initial transient (t<10s) consistent with electron trapping in the high-κ. Subsequently, the capped film has a higher defect creation rate.

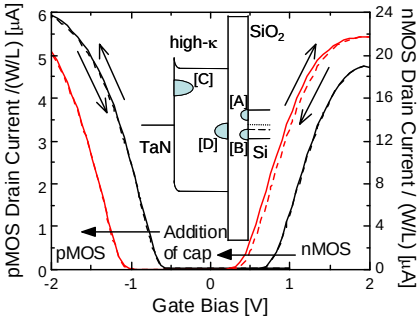

Figure 12. Hysteresis in long channel p and nMOS I_d-V_g characteristics shows electron trapping in capped nMOS devices. Defect profile in La_2O_3 capped dielectric bandgap shown in inset with defects at the Si/SiO_2 interface close to [A] $E_{c\ min\ Si}$, [B] $E_{v\ max\ Si}$, and in the high-κ, in the region close to the [C] MG/high-κ interface, and [D] SiO_2/high-κ interface.

References

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