## A-7-3

# Vertical Scaling of Metal/High-k Gate Stacked MOSFETs for Hp45 and Beyond

Takeo Matsuki, Toshinari Watanabe, Tetsu Morooka, Motoyuki Sato, Masaru Kadoshima, Takashi Onizawa, Takahisa Eimori, Mitsutoshi Nakamura, Yasuo Nara and Yuzuru Ohji

Semiconductor Leading Edge Technologies, Inc., 16-1 Onogawa, Tsukuba, Ibaraki, 305-8569, Japan Phone: +81-29-849-1187, FAX: +81-29-849-1186, e-mail: matsuki.takeo@selete.co.jp

#### **Abstract**

A specific issue in gate-poly-Si doping for deeply scaled poly-Si capped metal/high-k gate-first nMOSFETs was found that knock-on of metal element from gate electrode caused by a collision in As implantation leads to a degradation of gate dielectric reliability. By a careful tail profile design of the As implantation, a 20 nm gate length gate-first poly-Si/TaSiN/HfSiON nMOSFET with ~60-nm-gate height was successfully demonstrated with reliable gate dielectric characteristics.

#### **Introduction**

Si stacked high-k/metal gate system is a strong candidate for 32 nm technology node and beyond [1, 2]. The gate length scaling strongly needs the vertical scaling of both shorter gate height and deep source/drain (S/D) depth. The gate height scaling is required for robust manufacturing with scaled gate length and thus the aspect ratio of less than 3 should be maintained. For the metal/high-k planer MOSFETs, ion implantation process for gate and deep S/D should be taken care considering impurity penetration into both gate dielectrics/substrate and junction depth.

In this paper, a serious issue of degradation in gate dielectric reliability, which is particular to the Si-stacked metal/high-k gate, of gate dielectrics by S/D implantation is discussed. And a low energy As and P ion implantation technique is proposed with a successful demonstration of a vertically scaled high-k/metal/poly-Si nMOSFET which suppressed gate leakage current degradation associated with the S/D implantation.

#### **Experimental procedure**

A poly-Si/TaSiN/HfSiON/SiO<sub>2</sub> and poly-Si/HfSiON /SiO<sub>2</sub> gate nMOSFETs are prepared focusing gate-first MOSFET process. HfSiON, 2 ~ 2.5 nm, is formed with MOCVD and plasma nitridation following a high temperature annealing. A 10 nm TaSiN is deposited by PVD for the metal gate layer. The Si layer thicknesses are set at 50 nm on metal gate and at 75 nm in the case of poly-Si/HfSiON stack. After gate stack formation, gate doping and S/D formation with 1000°C spike annealing are performed in conventional self-aligned manner. The effect of As ion implantation energy for the gate doping and S/D formation in nMOSFETs was focused in this study. A W/TaSiN/HfSiON/SiO<sub>2</sub> stacked MOSFETs without gate doping are prepared.

#### **Results and discussion**

To simulate the gate dielectric degradation by implantation, 20 and 40 keV of the As implantation energy are selected using numerical process simulation (**Fig.1**). The 40keV-As collide with gate dielectric directly. Otherwise, the 20-keV-As does not collide with gate dielectric, but does collide with the TaSiN layer. The implanted As of the 20 keV-As in TaSiN is stopped at the surface region of the TaSiN, which is given by a Monte Carlo simulation (**Fig. 2**). Thus the 20 keV-As does not collide with the gate dielectric.

The gate leakage current (**Fig. 3**) and TDDB (**Fig. 4**) characteristics of n+-poly-Si/TaSiN/HfSiON/SiO<sub>2</sub>/n-Si gate stacked MOS capacitor is discussed to consider the effect of the As implantation on the electron gate leakage current. There is small observable difference in the leakage current

and TDDB life time of the 20/40 keV-As with poly-Si/HfSiON stack. This means that the direct collision of Ås with the HfSiON/SiO<sub>2</sub> gate dielectric does not have much impact on the reliability of the HfSiON/SiO<sub>2</sub> dielectric. However, in the poly-S/TaSiN/HfSiON/SiO<sub>2</sub>, the 40 keV-As implantation degrades both gate leakage and TDDB life time characteristics. This means that the implanted As ion with the energy of 40-keV possibly creates other degradation origin when the As travels through the TaSiN layer. The As ion travelling in the TaSiN layer collides with the element of TaSiN, and can knock on the element. The knocked-on elements, Ta, Si, and N, can be implanted into the HfSiON/SiO<sub>2</sub> dielectrics. Ta can increase leakage current [4]. Profile of the knocked-on Ta is evaluated by Monte Carlo simulation (Fig. 5). The 40 keV-As implantation can introduce Ta into the HfSiON/SiO<sub>2</sub> gate dielectrics with the knock-on process. The knocked-on Ta by the 20 keV-As, where the implanted As stops at the surface of the TaSiN layer, exists from surface of TaSiN to the end of the layer. This means that reaching of implanted As ion on to the TaSiN layer can degrade gate dielectrics reliability by its residual kinetic energy. And we must take a large margin to fix the implantation energy becoming lower. The lower As energy implantation requires thinner thickness of the Si layer or additional doping for the Si, to keeping high impurity concentration at the Si/gate metal interface and low contact resistance. A combination of low energy  $As^+$  and  $P^+$ implantation is a candidate to balance the trade-off [5]. However, the large diffusivity of P in Si has a risk of a short channel effect in deeply scaled MOSFET.

A combination of 5 keV for As<sup>+</sup> and 3 keV for P<sup>+</sup> is one of the lowest risk conditions for the degradations, and forms both highly-doped gate electrode and deep n-S/D (**Fig. 6**). Characteristics of scaled nMOSFETs (gate length: ~20 nm, EOT: ~1 nm) formed with Ni salicide are shown. Vt roll-off characteristics are summarized in **Fig. 7**. Id-Vg characteristics of 20 nm-gate length nMOSFET are successfully obtained with superior gate sheet resistance characteristics, <15  $\Omega$ /sq down to <30 nm gate length (**Fig. 8**, **9**, **10**). We confirm that favorable gate leakage and TDDB characteristics with a scaled HfSiON/SiO<sub>2</sub> gate dielectrics (EOT=1.1 nm) are obtained by using above condition (**Fig. 11, 12**).

### **Conclusion**

Higher sensitivity of As implantation energy toward the reliability of gate dielectrics was revealed in Si-stacked metal/high-k gate nMOSFETs. A vertical scaling of gate electrode considering the degradation of gate stack performance by S/D implantation has been found to be indispensable for cost-effective Si/metal/high-k MOSFETs with a successful demonstration using a low energy As<sup>+</sup>  $\mathbf{P}^+$ and S/D and gate implantation on poly-Si/TaSiN/HfSiON/SiO2 gate stacked nMOSFETs achieving 40 nm gate height and 20 nm gate length.

#### References

- [1] M. Chudzik et al., VLSI2007, p.194.
- [2] Y. Nishida et al, VLSI2007, p. 214.
- [3] H. Fukutome, et al., IEDM 2006, p.281.
- [4]Y. S. Suh et al, VLSI2001, p.47.
- [5] K. Imai, JJAP, p.2654 (2003)



Fig.1 Simulated profile of implanted As<sup>+</sup> in 75nm-thick poly-Si on HfSiON.



Fig.4 TDDB life time of soft breakdown with HfSiON (2.5 nm)/SiO<sub>2</sub>(0.7nm).



Fig. 7 Vt roll-off characteristics in various well doping condition. EOT=1.1 nm.









Fig. 5 Profile of knocked on Ta by As collision with a Monte Carlo simulation



Fig. 8 Id-Vg characteristics of Lg=20 nm nMOSFET. Well dope: B  $7x10^{12}$  cm<sup>-2</sup>.



Fig.11 Gate leakage current Jg vs EOT characteristics shows the As<sup>+</sup> 5keV& P<sup>+</sup> is enough for 1.0 nm era.



Fig. 3 Gate leakage current of poly-Si/HfSiON and n<sup>+</sup>-poly-Si/TaSiN/HfSiON with As<sup>+</sup> S/D implantation and spike annealing at 1000°C.



Fig. 6 Simulated high and low energy implanted As<sup>+</sup> and low energy implanted P<sup>+</sup> profile as implantation, and after spike annealing at 1000°C.



Fig. 9 Cross-sectional STEM images of nMOSFET with NiSi/Si/TaSiN/HfSiON/SiO<sub>2</sub>.



Fig.12 TDDB life time of soft breakdown of scaled gate dielectrics with HfSiON (2.5, 2.0 nm) /SiO<sub>2</sub>(0.7nm). EOT = 1.55 and 1.1 nm.