Vfb lowering effect of TaC/rare earth metal/TaC laminated gate electrode applicable to N-MISFET with HfSiON and its physical origins before and after high-temperature annealing

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1. Introduction
Rare earth metal (RE) incorporated metal gate (cap-metal/RE/TaC laminated gate or TaRE/RE/Caps) has been reported as a novel n-type metal gate electrode, because it offers lower flat-band voltage (Vfb) than that of TaC [1]. However, the physical origin of lower Vfb has not been fully investigated yet in the case of high-k gate dielectrics (HK). In this study, we investigate Vfb modulation of thermally stable TaC/HfSiON gate stack by inserting RE layer into TaC (TaC/RE/TaC laminated gate), changing annealing temperature (Tanneal) and HfSiON thickness systematically for physical understanding. We found that annealing temperature has a great impact on physical origin of Vfb modulation. TaC/RE/TaC shows lower Vfb compared with that of TaC before and after high-temperature annealing (HTA) owing to work function (WF) lowering of gate electrode and diffused RE near HfSiON/interfacial layer (I.L.) interface, respectively.

2. Experiment
TaC/HfSiON and TaC/RE/TaC(bottom-TaC)/HfSiON gate stacks were fabricated on p-type Si substrate to form capacitors (caps) as shown in Fig.1. TaC and RE were deposited by the sputtering method. Some of these samples were annealed at 700℃~1000℃ for 5sec in N2 atmosphere. The structure of gate stacks and the profiles of RE are identified by TEM-EELS, EDS and back-side (BS)-SIMS. All the samples went through forming gas annealing (FGA) at 450℃ for 30min before electrical measurements and physical analysis.

3. Results and Discussion
3-A. Before high-temperature annealing (HTA)
WF lowering of TaC by RE insertion:

Fig.2 shows the TEM image and the element profiles of TaC/Er/TaC/HfSiON stack after FGA (W/O HTA). Stack structure is almost the same as designed. However, as mentioned below (Fig.11), BS-SIMS revealed that a small amount of Er under the EDs detection limit (several atomic %) diffuses into bottom-TaC and HfSiON layer even before HTA. Fig.3 shows the Vfb dependence on Tphys (physical thickness) of gate dielectrics. Although Vfb for caps with HfSiON is 200mV higher than that with SiO2 in any conditions, implying the intrinsic dipole difference between metal gate (MG)/SiO2/Si and MG/HfSiON/I.L/Si stacks, almost the same Vfb shifts (~400mV) by Er are obtained regardless of the type and the thickness of gate dielectrics. It indicates that Vfb shift is due to WF lowering of gate electrode and not due to fixed charges or dipoles formed by diffused Er in gate dielectric. Two explanations of the WF lowering are proposed. One is that diffused Er in bottom-TaC reduces WF of MG. Actually, effective WF of TaC/Er formed by co-sputtering of TaC and Er (target composition is Ta:Er=7:3) is 500mV lower than that of TaC (Fig.4). It is thought to be due to the lower WF of Er than that of TaC. However, as described above, diffused Er in bottom-TaC is quite small (under several at.%), and so we still do not know if such a small amount of Er is enough for WF lowering of 400mV. The other explanation is the WF modulation effect of bi-metal layer. It has been reported that WF of bi-metal layer (MG, upper layer)/MG (lower layer in contact with gate dielectric) becomes near to that of MG when the thickness of MG2 is very thin (<2 nm) owing to the change of electron density resulting from WF difference between MG1 and MG2 [11]. Of course, it is possible that both of these physical origins contribute to the WF modulation.

Fig.5 shows the shift of effective WF (Φeff) on HfSiON by various types of RE. In all cases, Φeff of TaC/RE/TaC are comparable and lower than that of TaC. It is reasonable, since any RE has lower electron-negativities (χRE=1.1~1.2) than Ta and C (χTa=1.5, χC=2.5), which means WF of any RE is lower than that of TaC.

3-B. After high-temperature annealing (HTA)
Loss of the effect of lowered WF on Vfb shift:

Fig.6 shows Vfb dependence on Tphys of gate dielectrics after 1000℃ annealing. In the case of SiO2, Er lowers Vfb regardless of Tphys of gate dielectrics just like before HTA, and the value of Vfb shift (~400mV) is almost the same as that before HTA, which suggests that the effect of WF lowering on Vfb shift is maintained even after 1000℃ annealing. But for HfSiON, Vfb is lowered only when HfSiON is thin. Fig.7 shows Vfb-Tanneal plots for caps with thick HfSiON (7.0nm). There is no remarkable change of Vfb up to 700℃. However, above 800℃, the asymmetric Vfb shifts occur, which are Vfb lowering for TaC and Vfb increase for TaC/Er/TaC with higher Tanneal, resulting in loss of Vfb shift by Er compared with TaC. In Fig.8, thermal instability of Vfb for TaC/Er/TaC gated caps with HfSiON/I.L. is shown. HfSiON/SiO2 (3.0nm) and SiO2 are compared. Vfb is unstable when TaC/RE/TaC is in contact with HfSiON. This result implies that Vfb instability of TaC/Er/TaC gate is related to the interaction between gate electrode and HfSiON.

Appearance of another Vfb modulation effect by diffused Er:

Fig.9 compares Vfb-Tanneal plots of TaC/RE/TaC gated caps with thin (3.0nm) and thick (7.0nm) HfSiON. As described above, Vfb increases with higher Tanneal. However, in the case of thin (3.0nm) HfSiON, Vfb shows re-shift after 1000℃ annealing, resulting in lower Vfb compared with that of TaC again. Fig.10 shows that thinner HfSiON exhibits larger Vfb modulation effect. The dependence of the effect on HfSiON thickness indicates that diffused Er near HfSiON/I.L interface or at a closer point to Si substrate modulates Vfb, because the distance from RE layer to these points is decreased as HfSiON becomes thinner. In other words, the effects of diffused Er at the other point such as bottom-TaC or HfSiON layer must be obtained regardless of HfSiON thickness. BS-SIMS profiles confirm that Er piles up near HfSiON/I.L interface by 1000℃ annealing (Fig.11). Thus, the cause of Vfb shift after HTA is diffused Er near HfSiON/I.L interface.

Fig.12 shows Vfb of TaC and TaC/RE/TaC (RE:Y,La,Tb,Dy,Er) after 1000℃ annealing in the case of thick (7.0nm) and thin (2.3nm) HfSiON. Every RE lowers Vfb when HfSiON is thin (2.3nm), while caps with thick HfSiON (7.0nm) show no remarkable Vfb change by any RE. It implies that the above-mentioned explanation of Vfb modulation is applicable to all these REs. Quantitatively, these REs show a little difference. However these results are insufficient to compare ΔVfb among various types of RE being investigated.

4. Conclusion
We found that Vfb lowering of TaC/HfSiON by inserting RE layer into TaC (TaC/RE/TaC laminated gate) comes from the different physical origins before and after high-temperature annealing (HTA). Shown in Fig.13 are schematics illustrating the effect of RE on Vfb. Before HTA, Vfb shift into negative direction by the WF lowering of gate electrode is obtained, which is stable below 700℃ and is gradually lost at higher Tanneal above 800℃. After 1000℃ annealing, diffused Er near HfSiON/I.L interface shift Vfb into negative direction again resulting in lower Vfb compared with...
that of TaC. This effect and its physical origin are qualitatively common to various types of RE(Y,La,Tb,Dy,Er).

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Fig.1 The gate stack structures. (a)TaC-control, (b)TaC/RE/TaC
The thickness of RE and bottom-TaC are 2.5nm and 1.5nm, respectively.

Fig.2 (a)Cross sectional TEM image, (b)EELS(Hf,Ta,Er) and HAADF intensity depth profiles of TaC/Er/TaC(2.5nm)/HfSiON(1.5nm)/Si stack after FGA (W/O HTA).

Fig.3 Vfb and Tphys of gate dielectrics for TaC/Er/TaC capped SiO2 gate dielectrics after FGA(W/O HTA) as a function of Tphys of gate dielectrics.

Fig.4 Relationship between Vfb and Tphys of SiO2 gate dielectrics for TaC and TaErC gated caps with various structure of SiO2 gate dielectrics. ▲,△:TaC-control, ●,○:TaC/Er/TaC.

Fig.5 Changes in Vfb after annealing for (a)TaC-control, (b)TaC/RE/TaC.

Fig.6 Relationship between Vfb and Tphys of gate dielectrics for caps with thin(3.0nm) and thick(7.0nm) HfSiON after 1000 oC annealing followed by FGA.

Fig.7 The dependence of Vfb on Tannal for TaC and TaC/Er/TaC gated caps with thick(7.0nm) HfSiON.

Fig.8 Vfb instability of TaC/Er/TaC gated caps with various structure of gate dielectrics. ▲,△:Vfb after 1000 oC annealing followed by FGA(-)-Vfb after FGA.

Fig.9 Vfb, Tannal plots for TaC/Er/TaC gated caps with thin(3.0nm) and thick(7.0nm) HfSiON.

Fig.10 Relationship between ΔVfb and Tphys of HfSiON after 1000 oC annealing followed by FGA. ΔVfb=Vfb(TaC/Er/TaC)-Vfb(TaC).

Fig.11 Back-side SIMS Er profiles in TaC/Er/TaC/HfSiON stacks before HTA and after 1000 oC annealing. Both of the samples went through FGA.

Fig.12 Vfb of TaC and TaC/RE/TaC gated caps with HfSiON after 1000 oC annealing followed by FGA. (a)HfSiON=7.0nm, (b)HfSiON=2.3nm

Fig.13 Schematics illustrating the effect of RE on Vfb in the case of thin and thick HfSiON. (a) The image of RE distribution and its effect on Vfb before HTA and after 1000 oC annealing, (b) Vfb change with annealing temperature for TaC and TaC/RE/TaC gated caps with HfSiON.

References
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