Dual Metal Gate Technology with Metal Inserted FUSI Stack (MIFS) Using Single Phase FUSI for Scaled High-k CMOSFETs

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Abstract Dual metal gate technology with metal inserted FUSI stack (MIFS) is proposed for scaled high-k CMOS. A single Ni-rich fully-siliciuded (FUSI) layer is used for both FETs without forming two different FUSI phases and an ultra-thin TiN layer is selectively inserted between Ni-rich FUSI and high-k only in nFETs instead. Low effective work function (\(\phi_{\text{neff}}\)) of 4.45 eV is obtained by using MIFS with a structure of Ni-rich FUSI/ultra-thin TiN (~2nm) for nFETs. \(\phi_{\text{neff}}\) of Ni-rich FUSI fabricated after selective removal of TiN from HfSiON is as high as 4.8 eV for pFETs which is similar to that of control Ni-rich FUSI. Since \(V_{\text{FB}}\) remains unchanged when decreasing EOT, the dual metal gate technology is promising in scaled high-k CMOS from the viewpoints of \(\phi_{\text{neff}},\) process compatibility and EOT scaling.

1. Introduction

Metal inserted poly-Si stack (MIPS) gates with ultra-thin TiN (~2 nm) for nFET and with relatively thick TiN (~10 nm) for pFETs have been proposed as a possible solution for dual metal gates [1]. The combination of the fact that MIPS gates with ultra-thin TiN (~2 nm) and thick TiN (>10 nm) show different \(\phi_{\text{neff}}\) of ~4.45 and ~4.7 eV, respectively [1,2]. However, hole mobility (\(\mu_{h}\)) in pFETs, like electron mobility (\(\mu_{e}\)) in nFETs, tends to be slightly degraded with increasing the TiN thickness in MIPS. In this study, we investigate new dual metal gates without degrading \(\mu_{h}\) and with high compatibility to CMOS process. We select a metal-rich FUSI gate for pFETs that hardly suffers from the “pinning” problem on high-k. Metal inserted FUSI stack (MIFS: Ni-rich FUSI/TiN) gates are investigated for nFETs, because we expected that MIFS with ultra-thin TiN would have a low \(\phi_{\text{neff}}\) of ~4.45 eV on HfSiON like MIPS with ultra-thin TiN.

2. Experimental

HfSiON FETs with MIFS of Ni-rich FUSI/TiN and Ni-rich FUSI gates were fabricated. TiN was deposited on HfSiON(2.5 nm)/SiO\(_2\)(1 nm) by reactive sputtering. The thickness was set from 0 to 10 nm. 50 nm-thick poly-Si was deposited on TiN for MIFS or on HfSiON for Ni-rich FUSI by CVD. Spike annealing was carried out at 1000°C after gate patterning. Full silicidation was then carried out between the poly-Si and 100 nm-thick Ni at 450°C.

3. Results and Discussion

3.1 MIFS with ultra-thin TiN (UT-MIFS) for nFETs

The C-V curve in HfSiON nFETs is shifted towards the negative direction when the TiN thickness decreases from ~10 to 2 nm in MIFS (Fig. 1). The negative \(V_{\text{FB}}\) shift is quite similar to that for MIPS (Fig. 2). Furthermore, \(\mu_{h}\) is improved as the TiN thickness decreases from 10 to 2 nm in MIFS (Fig. 3). These clearly indicate that MIFS with ultra-thin TiN of about 2 nm (UT-MIFS) is advantageous for a metal gate in nFETs like MIPS with ultra-thin TiN.

According to the previous study for MIPS, the \(V_{\text{FB}}\) shift and change in \(\mu_{h}\) are ascribed to changes in the amounts of TiO(N) that acts like negative fixed charges or dipoles in the TiN/high-k interface [1]. The results for MIFS in Figs. 2 and 3 are consistent with the model because MIFS is just fabricated by full silicidation of poly-Si on TiN in MIPS.

On the other hand, \(V_{\text{FB}}\) is positively shifted when the TiN thickness decreases from 2 to 0 nm in MIFS (Fig. 1). The \(V_{\text{FB}}\) change for MIFS is the opposite direction of that for MIPS (Fig. 2). TEM and electron beam diffraction suggest that Ni-rich silicide with a Ni\(_{31}\)Si\(_{12}\) phase is formed on TiN in UT-MIFS as shown in Fig. 4(a). High \(V_{\text{FB}}\)s are observed in HfSiON pFETs by eliminating TiN in UT-MIFS, because UT-MIFS without TiN is Ni-rich FUSI that shows a high \(\phi_{\text{neff}}\) of ~4.8 eV on HfSiON owing to relaxation of the “pinning” for poly-Si by full silicidation to metal-rich silicide phase [3-5].

3.2 ultra-thin TiN-removed FUSI for pFETs

Compatibility of UT-MIFS with CMOS process is improved by simultaneously forming the Ni-rich silicide layer (Ni\(_{31}\)Si\(_{12}\)) both on ultra-thin TiN for nFETs and on high-k as the Ni-rich FUSI gate for pFETs. Therefore, it is required that ultra-thin TiN should be selectively removed from HfSiON only in pFET area.

A Ni\(_{31}\)Si\(_{12}\) phase and no residue of TiN are observed in Fig. 4(b) after removing 2 nm-thick TiN from HfSiON by H\(_2\)O\(_2\)/H\(_2\)O. By removing 2 nm-thick TiN, the C-V curve is positively shifted by 0.35 V without a distinct EOT increase (Fig. 5). \(V_{\text{FB}}\) for Ni-rich FUSI formed after removing 2 nm-thick TiN is almost the same as that for control Ni-rich FUSI which is shown as MIFS with 0 nm-thick TiN in Fig. 6. \(\mu_{h}\) for TiN-removed Ni-rich FUSI is as high as that for UT-MIFS (Fig. 7). No “\(V_{\text{FB}}\) roll-off” is observed and high mobility is maintained when we apply the UT-MIFS and Ni-rich FUSI gates into HfSiON FETs with a thinner EOT of ~1.2 nm (Figs. 8 and 9). \(|V_{\text{t}}|\) is actually reduced by 0.34 V in HfSiON pFETs by changing the gate structure from UT-MIFS to TiN-removed Ni-rich FUSI (Fig. 10).

The dual metal gates proposed in this study are summarized in Fig. 11. A single Ni-rich FUSI phase is used for both FETs and an ultra-thin TiN layer is selectively inserted between Ni-rich FUSI and HfSiON only in nFETs. The boundary is clearly determined by the edge of the ultra-thin TiN. HfSiON FETs are fabricated with TiN, TiN-removed Ni-rich FUSI, and Ni-rich FUSI gates into HfSiON FETs with a thinner EOT of ~1.2 nm (Figs. 8 and 9). \(|V_{\text{t}}|\) is actually reduced by 0.34 V in HfSiON pFETs by changing the gate structure from UT-MIFS to TiN-removed Ni-rich FUSI (Fig. 10).

4. Conclusion

Dual metal gate technology with UT-MIFS of Ni-rich FUSI/ultra-thin TiN for nFETs and Ni-rich FUSI for pFETs has been demonstrated. The dual metal gates are simultaneously fabricated only by adding simple steps of selective ultra-thin TiN insertion in nFETs to a single metal gate process with Ni-rich FUSI. The TiN edge determines the boundary precisely. The technology has scalability for 32 nm high-k CMOS and beyond.


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Fig. 1 C-V curves of HfSiON nFETs with MIFS. Labels denote the TiN thickness in MIFS. The curves are shifted by changing the TiN thickness.

(a) UT-MIFS (TiN 2nm)  (b) TiN-removed Ni-rich FUSI

Fig. 4 TEM images of (a) UT-MIFS with 2 nm-thick TiN and (b) Ni-rich FUSI gates formed after removing 2 nm-thick TiN. Same Ni$_{31}$Si$_{12}$ phase is formed on both (a) TiN and (b) HfSiON.

Fig. 7 $\mu$ and EOT as functions of the TiN thickness. High $\mu$ is observed when using Ni-rich FUSI formed after removing 2 nm-thick TiN.

Fig. 10 $I_{D}$-$V_{G}$ curves of HfSiON FETs. $V_{T}$ is lowered by 0.34V in pFET by changing UT-MIFS to TiN-removed Ni-rich FUSI.

Fig. 2 $V_{FB}$ and EOT as functions of the TiN thickness. Labels indicate the thickness. $V_{FB}$ is negatively shifted by changing the thickness from 10 to 2 nm for both MIFS and MIPS.

Fig. 8 $V_{FB}$ and $\mu$ vs. EOT for UT-MIFS gate HfSiON nFET. $V_{FB}$ remains unchanged when EOT is reduced to 1.2nm (no “$V_{FB}$ roll-off”).

Fig. 9 $V_{FB}$ and $\mu$ vs. EOT for Ni-rich FUSI HfSiON pFET. $V_{FB}$ remains unchanged when EOT is reduced to 1.2nm (no “$V_{FB}$ roll-off”).

Fig. 11 Dual metal gates proposed in this study. These are fabricated by inserting ultra-thin TiN on high-k only in nFET and by forming Ni-rich FUSI both in n and pFETs simultaneously. The boundary between UT-MIFS and Ni-rich FUSI is clearly determined by the TiN edge. $\phi_{m,eff}$s are 4.45 and 4.8eV on HfSiON. Band edge $\phi_{m,eff}$s are expected to be obtained by combining dual high-k technique.