Hybrid Gate Structures of NMOS : Poly-Si / PMOS : 2 Layers Ni-FUSI by using Flash Lamp Anneal (FLA) and CMP

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Abstract
We applied Flash Lamp Annealing (FLA) in gate Ni-silicidation and Chemical Mechanical Polish (CMP) to conventional structure for the first time. For pMOSFET, 2 layers Ni Fully-silicide (Ni-FUSI) was selectively formed on gates, and both off-state leakage currents and drive currents are improved. On the other hand, unlike pMOS, Ni-FUSI process is not performed in nMOS. Consequently, nMOS performance are almost the same. pMOS drive current enhancement of 32 % was achieved, attributed to the thinner equivalent oxide thickness of inversion layer capacitance (\(T_{\text{eff}}\)) and possibly gate silicide strain effects for pMOS. We successfully formed the hybrid gate structures.

Introduction
FUSI gate is a promising technology to improve device performance [1-3]. We have already reported the most effective solution, named as Melt-FUSI [4]. This FUSI using FLA has advantages that 1) TDDB reliability is better than control, 2) the hole mobility is improved. However, this integration flow have a problem that FUSI gate depend in a large part on gate length. In this paper, we present the process feasibility, gate length dependence and superior electrical characteristics of 2 layers Ni-FUSI pMOSFETs using CMP + FLA.

Results and discussion
Figure 1 shows the integration flow using CMP + FLA of pMOSFET. Gate electrode structure is 2 layer structures (NiSi/NiSi2). After S/D region was implanted, dopant was activated using spike anneal. The process is identical to the standard CMP flow up to the S/D annealing after which a hard mask is deposited. After a disposable hard-mask layer deposition the gate was subject to a CMP process to expose the gate poly-Si. Ni-mono-silicide (NiSi) was formed on the gate using 1st-silicide annealing. After the disposable hard-mask layer was removed, Ni silicide (NiSi2) was formed using FLA for 2nd-silicide annealing. Following this step, Ni-mono-silicide (NiSi) is formed on the gate and S/D by using conventional method.

Figure 2 shows cross-sectional TEM images of pMOS after full processing. It is clearly observed that the gate electrode is 2 layer structures (NiSi/NiSi2). We have already investigated Ni-FUSI phases using FLA [4]. The \(V_{\text{th}}\) shifts of pMOS are 190 mV while C-V characteristics of nMOS are almost the same (Fig. 3). The 2 layers Ni-FUSI process increased the maximum \(C_{\text{gs}}\) by 8% for pMOS. In this work, gate oxynitride is used, with achieving the equivalent oxide thickness of inversion layer capacitance (\(T_{\text{eff}}\)) = 5.31 nm and 5.36 nm by 2 layer structures for nMOS and pMOS, respectively. We successfully eliminated the gate depletion effect of pMOS. Fig. 4 shows saturation threshold voltage roll-off of nMOS and pMOS respectively. It is clearly observed that Vth of pMOS shifted toward the negative direction throughout a range of Lgate. It is known this method have little influence over gate length. On the other hand, unlike pMOS, Ni-FUSI process is not performed in nMOS. Since excellent uniformity and lower gate sheet resistance, low junction leakage, little gate length dependence and the process simplicity are achieved, we propose that this 2 layers Ni-FUSI process can be a standard for 32 nm technology and beyond.

Figure 6 shows \(I_{\text{on}}\)-\(I_{\text{off}}\) characteristics of pMOSFETs. The \(I_{\text{on}}\) of Ni-FUSI improved by 32 % compared to the control device (without Ni-FUSI). Additionally, improvement of off-state leakage currents were achieved. The drive current enhancement of 32 % was achieved, attributed to the thinner equivalent oxide thickness of inversion layer capacitance (\(T_{\text{eff}}\)) and possibly gate silicide strain effects for pMOS. Fig. 7 shows liner drive current vs off-leakage current characteristics of pMOS at \(|V_{\text{dd}}|=0.1\ V\). The liner drive current of FUSI improved by 50% compared to the control device (without FUSI). Fig. 8 shows \(I_{\text{d}}-V_{\text{th}}\) characteristics of a FUSI device using FLA + CMP and a control device at off-state leakage current of 100 pA/\mu m. There are a 32 % drive current and a 50 % liner drive current improvement with FUSI. Well controlled sub-threshold slope of 73.7 mV/dec and 81.5 mV/dec were obtained for gate length 190 nm nMOS and pMOS, respectively (Fig. 9). Highest Ion of 802 \mu A/\mu m for nMOS and 551 \mu A/\mu m for pMOS at \(|V_{\text{dd}}|=1.8\ V\ were obtained. N+/p junction leakage current and its distribution results are shown in Fig. 10. No increase of junction leakage current and tight distribution are observed in the monitor of perimeter contacts. Fig. 11 shows the measured gate sheet resistance and its distribution in gate length 30nm Tr. As can be seen, it did not trigger silicide problems. The lower sheet resistance is obtained by the 2 layer structures. It is known that NiSi2 sheet resistance became unacceptably high. The use of the 2 layers (NiSi/NiSi2) realizes low sheet resistance of gate and thinner \(T_{\text{eff}}\). Table 1 shows the device performance summary in this work. Table 1 shows the material of gate electrode, \(\delta V_{\text{th}}, \) Ion improvement, Idlin improvement, \(T_{\text{eff}}\) Roll-off improvement, Junction leakage and Gate sheet resistance for nMOS and pMOS, respectively.

Conclusions
We applied FLA in gate Ni-silicidation and CMP to CMOSFETs for the first time. For pMOSFET, 2 layers Ni-FUSI was selectively formed on gates, and both off-state leakage currents and drive currents are improved. In addition, this method have little influence over gate length. On the other hand, unlike pMOS, Ni-FUSI process is not performed in nMOS. Since excellent uniformity and lower gate sheet resistance, low junction leakage, little gate length dependence and the process simplicity are achieved, we propose that this 2 layers Ni-FUSI process can be a standard for 32 nm technology and beyond.

References
Fig.1 Integration flow using CMP+FLA of pMOS. Gate electrode is 2 layer structure (NiSi/NiSi$_2$).

Fig.2 TEM cross sections of pMOS. Ni-FUSI was selectively formed on pMOS. Gate electrode is 2 layer structure (NiSi/NiSi$_2$).

Fig.3 Effects of FLA in Ni-silicidation on gate capacitance. 2 layers Ni-FUSI with Vfb shift was selectively formed on pMOS.

Fig.4 Saturation threshold voltage roll-off of nMOSFETs and pMOSFETs respectively.

Fig.5 Liner drive current vs off-leakage current characteristics of nMOSFETs at $V_{dd}$=1.8V. Ion improves (+50%) by 2 layers Ni-FUSI using CMP+FLA.

Fig.6 Drive current vs Off-leakage current characteristics of pMOSFETs at $V_{dd}$=1.8 V. Ion improves (+32%) by 2 layers Ni-FUSI using CMP+FLA.

Fig.7 Liner drive current vs off-leakage current characteristics of pMOSFETs at $V_g$=1.8 V. Idlin improves (+50%) by 2 layers Ni-FUSI using CMP+FLA.

Fig.8 Id-Vd characteristics of 2 layers Ni-FUSI using CMP + FLA and a control device. The highest drain current of 551 μA/μm was obtained for pMOS.

Fig.9 Subthreshold Id-Vg performance of gate length 190 nm nMOS and pMOS respectively. Well controlled sub-threshold slope of 73.4/81.5 mV/dec were obtained.

Table 1 Device performance summary in this work. Table 1 shows the material of gate electrode, $d$Vth, Ion improvement, Idlin improvement, Toff. Roll-off improvement, Junction leakage and Gate sheet resistance for nMOS and pMOS, respectively.

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<thead>
<tr>
<th>CMP + FLA</th>
<th>nMOS</th>
<th>pMOS</th>
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<tbody>
<tr>
<td>Gate electrode</td>
<td>Ni-silicide/Poly</td>
<td>2 layers Ni-FUSI</td>
</tr>
<tr>
<td>$d$Vth</td>
<td>900mV</td>
<td>1900mV</td>
</tr>
<tr>
<td>Ion</td>
<td>No change</td>
<td>+32%</td>
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<tr>
<td>Idlin</td>
<td>No change</td>
<td>+50%</td>
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<tr>
<td>Toff.</td>
<td>5.31nm</td>
<td>5.36nm</td>
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<tr>
<td>Roll-off</td>
<td>No change</td>
<td>Improvement</td>
</tr>
<tr>
<td>Junction Leakage</td>
<td>No change</td>
<td>No change</td>
</tr>
<tr>
<td>Sheet Resistance</td>
<td>Improvement</td>
<td>Improvement</td>
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