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Carbon-Free Tantalum-Nitride Film from Ammonia and Extremely Diluted Pentakis-dimethylamino-Tantalum; Effect of Silicon Incorporation to nMIS-FET Metal-Gate

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1. Introduction

Tantalum-nitride (TaN) is a promising material as a metal gate-electrode of future MIS-FET because of its chemical stability, diffusion barrier property and robustness against high temperature Si-LSI process (950-1050^{o}C). The effective workfunction of TaN is corresponding to the mid gap of Si (~4.6eV). As a result, $TaSi_xN_y$ compound is usually used to n-MOS-FET applications as a conduction-band-edge workfunction metal because the Si incorporation lowers the film workfunction [1]. On the other hand, electron mobility degradation is a typical problem of metal-gate transistors. We found that the incorporation of Si into TaN also improves electron mobility in a Hf-based high-k (high dielectric constant gate-dielectrics) metal-gate transistor. In this paper, the mechanism of mobility improvement during Si incorporation is discussed comparing the results with TiN or $TiSi_xN_y$ gate devices.

It is known that the chemical vapor deposition (CVD) of TaN is difficult because of the luck of appropriate CVD precursors. Most of source-materials such as halides show very low vapor-pressure and halogen incorporation problem. Typical high vapor-pressure metal-organic (MO) precursors give rise to severe carbon incorporation during CVD. We have established an MOCVD technology for carbon-free TaN and $TaSi_xN_y$ films using with NH_3, Pentakis-Di-Methyl-Amino-Tantalum (PDMAT; $Ta[N(CH_3)_2]_5$) and Si_2H_6. This technology does not require any plasma assistance. Deposition chemistry is also described concerning with vapor-phase reaction of these materials.

2. Experiments

CVD TaN was thermally deposited from NH_3 and PDMAT at the temperature ranging from 350^{o}C to 500^{o}C. PDMAT is solid low vapor-pressure material (Fig. 1). A special precursor bottle designed for solid material was used for stable source delivery and the partial pressure of PDMAT in carrier gas (Ar) was monitored by a supper-sonic flow meter. $TaSi_xN_y$ films were prepared by the alternating deposition of CVD TaN-layers and Si-layers from Si_2H_6. Typical sub-layers depositions were about 0.5nm for the each material with a total metal gate thickness of 10nm. High-k MIS-FETs were fabricated with a conventional gate-first process. The wire-metal was 50nm W. The gate dielectric was 2.5nm HfSiON giving an effective-oxide-thickness (EOT) of 1.1nm [2, 3]. Activation temperatures after gate-formation were 850-1000^{o}C. TiN and TiSiN metal-gate transistors were fabricated with the same process. The TiN and TiSiN metal-gates were deposited by sputtering method (PVD).

3. Results and Discussion

In Fig. 2, the growth temperature dependences of Carbon and hydrogen residence in CVD-TaN, measuring by SIMS, were shown. Both the C and the H residence was extremely low (<0.5%) and those were decreased with the decreasing of the growth temperature. It was also confirmed that any thermal decomposition of PDMAT, without NH_3, provides TaCN film (C: ~30%). The results suggest the deposition of a carbon-free TaN film does not require thermal assistance, with all organic ligands of PDMAT being eliminated by NH_3 with high efficiency. Conventional reaction model of PDMAT and NH_3 involves a subsequent substitution reaction, with the elimination of five-ligands from PDMAT requiring five time fold substitution with NH_3. This does not realistically explain our results. We suppose, however, that the NH_3 can decompose PDMAT and create carbon-free Ta-fragment with one reaction. It must be also emphasized that the partial pressure of PDMAT was 10^{-5} Torr under our deposition condition and the vapor phase reaction between PDMAT and its fragment could thus be negligible. We can conclude that the vapor phase reaction between NH_3 and extremely diluted PDMAT can provide carbon-free TaN film.

As shown in Fig. 3, the film composition can be changed with wide rage by the alternating deposition of TaN and Si. Effective workfunction estimated from CV characteristics (Fig. 4) decrease with the increase of Si composition in the films. The electron mobility of high-k/metal-gate transistors was improved with the increase of Si incorporation, as shown in Fig. 5. We found the similar phenomena with TiN or $TiSi_xN_y$ gate transistor, as seen in Figs. 6 and 7. It is noticeable that the recovery of mobility accompanied with workfunction decreasing, with different gate-material or different gate-process transistor.

With Hf-based high-k transistor, Fermi-level-pinning is the biggest problem, especially when high temperature process is employed. The pinning position is thought to be at ~4.3eV and it is believed that the pinning is caused by some charge transfer between gate-metal and gate-dielectrics accompanied by some elemental transfer (e.g. O) during high temperature process [4]. Such charge transfer might degrade the channel mobility of high-k/metal-gate transistor. When the original workfunction of gate material is closed to be 4.3eV, any charge transfer would not be possible. We consider that Si incorporation into gate-metal might suppress the portion of charge transfer related to the Fermi-level-pinning at high temperature, as shown in Fig. 8. The model suggests that the best workfunction is ~4.3eV for n-MIS gate material.

4. Conclusion

A carbon-free MOCVD TaN film was prepared by the vapor phase reaction between NH_3 and extremely diluted PDMAT. Si incorporation into the film provided good effective workfunction as n-MIS gate material. The Si incorporation also improved the channel mobility of Hf-based high-k MIS-FETs. It was noted that the mobility degradation in the high-k/metal-gate transistor could be related to the Fermi-level-pinning of Hf-based high-k dielectrics which modify the effective workfunction of gate-metal.

References

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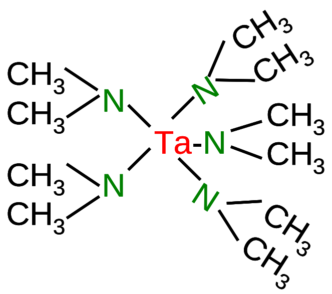

PDMAT
(Pentakis-dimethylamino-tantalum)
$Ta[N(CH_3)_2]_5$

Melting point: >150°C
Sublimation pressure: 80°C/0.1Torr

Fig. 1 Structure of PDMAT

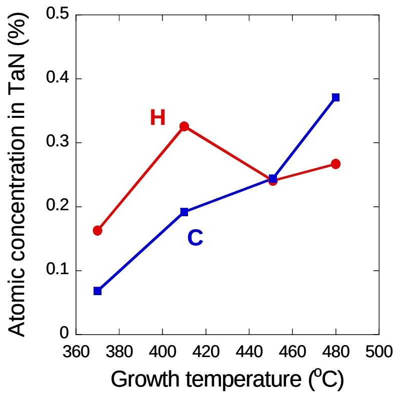

Fig. 2 Growth temperature dependence of impurities in CVD-TaN film. Both C and H were measured with SIMS.

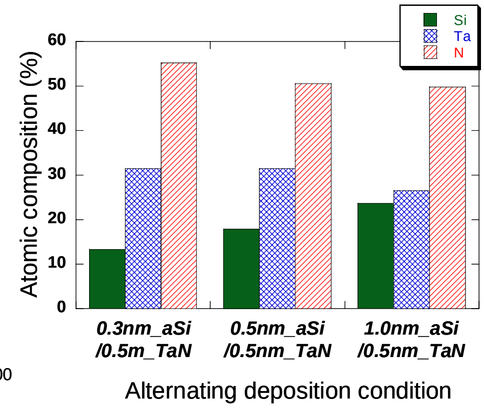

Fig. 3 Control of composition by alternating deposition of TaN-layers and Si-layers. Typical sub-layer thickness was 0.5nm. TaN-layer was deposited from NH_3 and PDMAT. Si-layer was deposited from Si_2H_6.

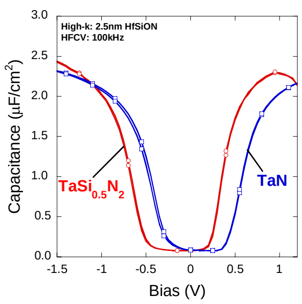

Fig. 4 High frequency capacitance-voltage characteristics of TaN or TaSiN metal-gate transistors. Gate dielectrics were 2.5nm HfSiON. TaN and TaSiN gate were prepared with MOCVD.

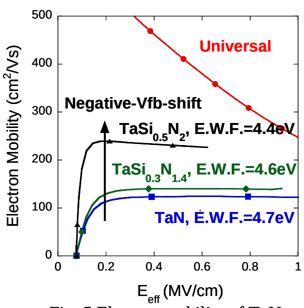

Fig. 5 Electron mobility of TaN and TaSiN gate transistors. Gate dielectrics were 2.5nm HfSiON.

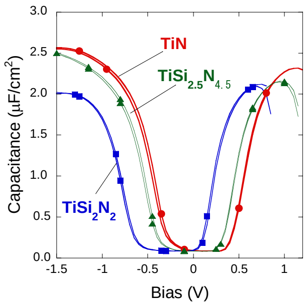

Fig. 6 High frequency capacitance-voltage characteristics of TiN or TiSiN metal-gate transistor. Gate dielectrics were 2.5nm HfSiON. TiN and TiSiN were prepared with magnetron sputtering.

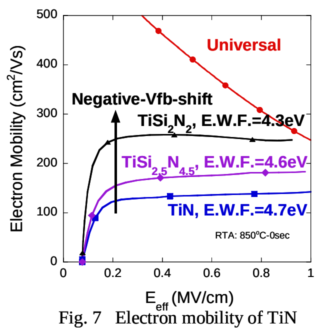

Fig. 7 Electron mobility of TiN and TiSiN gate transistors. Gate dielectrics were 2.5nm HfSiON.

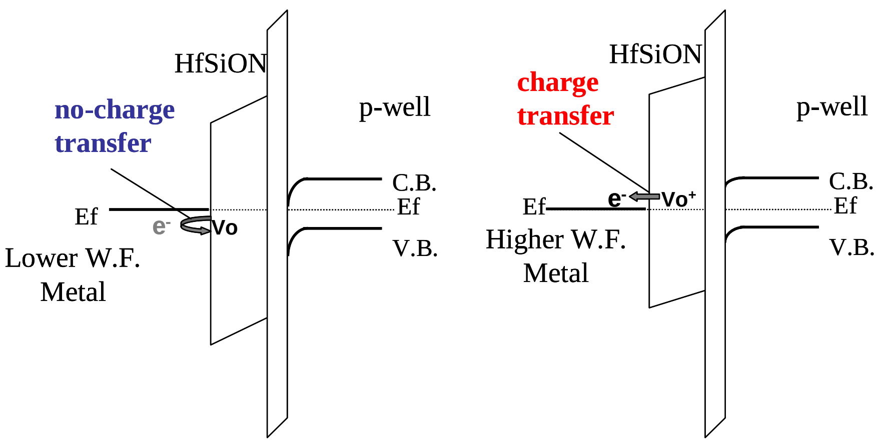

Fig. 8 Band diagram of a charge transfer model for n-MIS-FET. In this model, charge transfer from gate dielectric depends on the Fermi level of gate-metal. In the case of higher work-function gate (>4.3eV), electron-transfers from Hf-based high-k occur in a thermo-dynamical equilibrium condition. This is well-known Fermi-level-pinning model. When the gate-metal has the same work-function energy as the pinning position (~4.3eV), charge transfer does not occur. The charge in the dielectric would be minimized and the channel mobility would thus be recovered.