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III-V CMOS: Challenges and Opportunities

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1. Introduction

The microelectronics revolution is now nearly 50 years old. For all this time, its rallying cry has been "*Smaller is Better,*" the expectation that transistor size scaling brings along exponential improvements in transistor density (and cost), performance (switching speed) and power consumption. Yet, in its middle age, the concerns for its long term health are mounting. Si-based CMOS scaling appears to be running into very serious technological barriers. With a development cycle that spans about 10 years before a new technology node can be brought to production, it is imperative to immediately start exploring alternative options to Si-based CMOS. This talk will review the opportunities to be found in the extraordinary properties of III-V compound semiconductors and the challenges that are faced before III-V CMOS can become a reality. Could III-V's herald a Golden Age for the microelectronics revolution?

2. The case for III-V CMOS

At the heart of the problems that Si faces is the fact that as transistor size scales down, the ratio of intrinsic gate capacitance to parasitic capacitance continues to decrease [1]. In effect, with each generation, the "dead weight" that the transistor needs to carry keeps increasing in relative terms. Since transistor density is the number 1 goal of the industry, it is inevitable that power consumption and switching speed will eventually suffer.

A way out of this is possible if the current drive could be improved through a higher carrier velocity in the channel. This is precisely where III-Vs excel, at least for electrons. With inversion layer electron mobilities that span anywhere between about 7,000 and 30,000 $cm^2/V.s$ at room temperature, III-Vs promise substantial enhancements in current drive and switching speed at a reduced operating voltage. To be sure, mobility is not the same as velocity. However, carrier mobility and the source injection velocity, which is what matters in a nearly ballistic logic FET, have been found to be strongly correlated to each other [1]. A manifestation of the intrinsic superiority of III-Vs as it comes to performance is the record frequency response of III-V based transistors when compared with their Si-based counterparts which has lasted for at least 20 years.

In addition to these intrinsic advantages, III-V electronics has achieved a reasonable level of maturity in both manufacturing and reliability, with many systems having been deployed in critical applications including in space.

3. The "Grand Challenges" of III-V CMOS

What stands on the way of the development of III-V CMOS? There are at least five grand challenges that need to be overcome. They are summarized in Fig. 1.

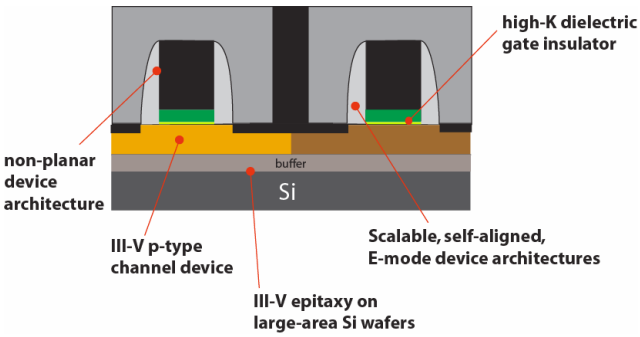

Fig. 1: "Grand Challenges" of III-V CMOS.

First, one has to demonstrate high quality epitaxial growth of III-V heterostructures on very large Si wafers with very thin buffer layers (for thermal reasons, but also for manufacturing cost reasons). It stands to reason that a post-Si CMOS technology better leverage the enormous investment in manufacturing capacity and tool development that will exist at the time of its deployment. In effect, this new technology has to "look and feel" as much like Silicon as possible.

In order to meet the density requirements of the 15 nm node, exceptional electrostatic integrity will be essential. This will demand the development of MIS-type FETs with a thin and reliable high-k dielectric barrier material. In turn, this will require tackling what is probably the hardest problem of all, avoiding Fermi level pinning and obtaining a high quality passivated III-V surface that approaches the quality of the SiO_2/Si system.

In addition, future III-V enhancement-mode FETs are needed with a self-aligned device architecture for minimum footprint and parasitics.

A future III-V CMOS logic technology might also require 3D-type device structures, such as Fin-FET or triple gate, something never quite demonstrated with III-V's.

Finally, one will have to contend with the poor hole mobility. Here the hope is that, similar to Si and Ge where enhancements as high as 5X have been demonstrated, the introduction of strain will allow us to engineer the valence band so as to boost the hole mobility.

4. What can we learn from III-V HEMTs?

In our quest to demonstrate III-V CMOS, the HEMT represents an invaluable "model device." The HEMT is in its own right an FET with a "medium-k" gate barrier. However, due to gate leakage current, it is not expected to scale down to the dimensions that are required. Nevertheless, the HEMT is an excellent test bed for new III-V device design concepts that are essential, such as self-alignment techniques (Fig. 2 [2]), novel ohmic contacts, novel isolation schemes, and new approaches to produce enhancement-mode transistors.

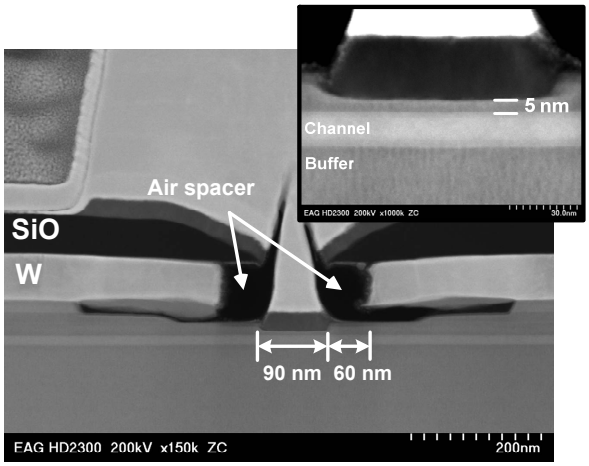

Fig. 2: Cross-section of fabricated 90 nm self-aligned enhancement-mode InGaAs HEMT [2]. The source and drain electrodes are located 60 nm away from the gate edge.

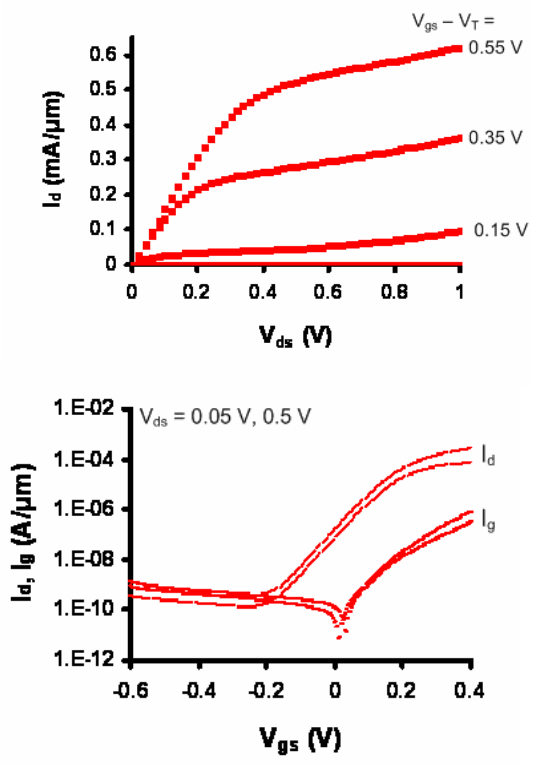

Fig. 3: Output and subthreshold characteristics of the 90 nm InGaAs HEMT shown in Fig. 2 [2].

In addition, the HEMT is a superb test bed to investigate device physics of relevance to future high-k III-V FETs such as the impact of the low density of states characteristic of III-Vs, scaling characteristics of all parasitic resistance and capacitance components, the impact of strain on transport physics, and the impact of low bandgap on band-to-band tunneling in the channel.

Finally, the HEMT is a model device that allows us today to start developing and calibrating the device simulators that will be required in the future.

5. How good are III-V HEMTs for logic?

In communications systems, the domain in which III-V HEMTs excel, these devices are mostly used as amplifiers. When an FET operates in a logic circuit, it really behaves like a switch. The relevant figures of merit are not f_T or f_{max}, but rather switching delay, subthreshold swing, ON-OFF ratio and V_T and its dependence on geometry and operating voltage, among others. It has been a pleasant surprise to realize that modern III-V HEMTs actually exhibit excellent logic characteristics. Sub-100 nm InGaAs HEMTs have been demonstrated with current drive, ON/OFF ratios, and short-channel effects that rival those of state-of-the-art Si transistors at significant lower operating voltages [3-7]. Recently, 30 nm HEMTs with a very thin channel that includes a pure InAs layer have shown exceptional logic characteristics as well as a world record f_T [7].

The excellent logic characteristics that HEMTs have demonstrated have energized the field. In a way, they represent a high-water mark that we now know future high-k/III-V FETs ought to be able to achieve.

6. Conclusions

Among the alternatives to Si CMOS, III-Vs look promising. III-V electronics is a real technology with a proven track record in mission critical communication systems. Recent research on HEMTs shows that excellent logic performance is possible at dimensions that approach those of future logic devices.

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