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B-1-2

Enhancement-Mode $In_{0.53}Ga_{0.47}As$ n-MOSFET with Self-aligned Gate-first Process and CVD HfAlO Gate Dielectric

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Abstract

This work reports the demonstration of enhancement-mode $In_{0.53}Ga_{0.47}As$ n-channel MOSFET using HfAlO gate dielectric and TaN metal gate using a self-align process for the first time. We employ the conventional self-aligned gate-first process with low temperature dopant activation. The incorporation of Indium in InGaAs channel not only provides higher electron mobility but also improves interface quality with high-k dielectric, enabling direct deposition of HfAlO on InGaAs channel. Source and drain dopant activation can be achieved at low temperature (600 ^{o}C) with excellent junction property.

Introduction

With the scaling of Si-based MOSFET reaching its fundamental limits, considerable interest has been directed toward channel engineering using high electron mobility III-V materials such as GaAs. GaAs n-MOSFET with Si passivation layer has been demonstrated [1]. Comparing to GaAs, ternary III-V compound InGaAs can be a better candidate as n-channel materials because of its higher intrinsic electron mobility (x9 Si for Indium 53%), better interfacial integration with high-k dielectric than GaAs, lower temperature for dopant activation, larger Γ-L valley difference and the feasibility for bandgap engineering. Recently, $In_{0.53}Ga_{0.47}As$ n-MOSFET employing the gate-last process was fabricated and exhibited high electron mobility [2, 3].

This work, for the first time, demonstrates the enhancement mode $In_{0.53}Ga_{0.47}As$ n-channel MOSFET using a self-aligned process, and the feasibility of using low temperature implantation activation. The low temperature activation is associated with the high concentration of Indium, leading to excellent junction meanwhile maintaining good high-k/ semiconductor interface.

Device Fabrication

A self-aligned n-MOSFET fabrication process is employed as shown in Fig. 1. Fig. 2 shows the schematic cross section of device structure. Starting from a P^{+} InP wafer, approximately 200 nm buffer InP and 500 nm lattice-matched $In_{0.53}Ga_{0.47}As$ (InGaAs for short) is grown by MBE subsequentially. Indium percentage is confirmed by HR-XRD. P-type dopant is Zn and carrier concentration in the buffer InP and InGaAs epi-layer was studies by an electrochemical capacitance-voltage (ECV) profile in Fig. 3. Concentration is $1x10^{17}$ cm^{-3} near the surface. HCl pre-cleaning and $(NH_4)_2S$ surface treatment is applied before the high-k deposition. AFM images in Fig. 4 show the surface roughness before (a) and after (b) this step. The surface roughness is slightly increased by using this chemicals treatment. Immediately after that, the HfAlO consisting of 90% HfO_2 and 10% Al_2O_3 is used as gate dielectric, which is directly deposited by $(HfAl(MMP)_2(OiPr)_5)$ source, and followed by the *in-situ* PDA at 500 ^{o}C for 30 s. Reactive sputtering TaN gate electrode is deposited and patterned. S/D is implanted with Si by 50 KeV/$1x10^{14}$ cm^{-2}. Implantation activation is achieved by RTA at 600 ^{o}C for 60 s in N_2 ambient. AuGe/Ni/Au and Ti/Pd/Au are deposited to form front S/D contact and backside contact, respectively, followed by RTA at 360 ^{o}C. Lastly, the forming gas annealing is performed at 400 ^{o}C for 60 s.

Results and discussions

XPS is used to compare the GaAs and InGaAs interface quality with HfAlO. The de-convoluted O 1s spectra from HfAlO/GaAs and HfAlO/InGaAs in Fig. 5 clearly show that the incorporation of Indium can effectively suppress the formation of GaO and AsO at the interface after the HfAlO growth. HRTEM image in Fig. 6 illustrates excellent interface between MOCVD HfAlO and InGaAs. HfAlO film thickness is 14.1 nm. Fig. 7 shows excellent capacitances in an InGaAs n-MOSFET. The C-V characteristic between gate and substrate fits well with the simulated curve with a sharp transition and good accumulation behavior, indicating an excellent interface with low trapping density and Fermi level pinning free interface. The C-V characteristic between gate and tided-up S/D shows excellent inversion characteristics for MOSFET turn on operation. The EOT of HfAlO film in this work is estimated to be 4.46 nm by fitting with the simulated curve considering quantum mechanical effects. Fig. 8 shows extremely low leakage currents of TaN/ HfAlO/ InGaAs gate stacks for both gate and substrate injection cases, which can be attributed to the high conduction band offset (CBO) and valence band offset (VBO) between HfAlO and InGaAs channel [5].

Low temperature process is desirable for high-K/high-mobility channel system in order to mitigate the constraints of their thermal stability issues. RTA temperatures for dopant activation from recently reported GaAs and gate-last InGaAs transistors are normally above 750 ^{o}C [1-4]. InGaAs transistor in this work utilizes a RTA temperature of 600 ^{o}C and it is sufficient to obtain excellent activated S/D junctions with 6 orders of rectifying characteristic at ±1 V (Fig. 9) and low sheet resistivity.

Fig. 10 illustrates the I_d-V_d characteristic of InGaAs n-MOSFET for varying gate bias. For V_g of 4 V and V_d of 4.5 V, the transistor with gate length of 4 μm provides a drain current density of 56 mA/mm. At V_g of 0 V the transistor is well turned off, indicating excellent enhancement mode performance. I_d-V_g and G_m-V_g characteristic of the InGaAs n-MOSFET with W/L=800/4 μm biased at different V_d are shown in Fig. 11. The threshold voltage is extracted to be 0.2 V and the maximum transconductance is 22 mS/mm. The inset of Fig. 11 shows the subthreshold performance of the device at a drain bias of 1 V. On/off current ratio is in 4 orders at room temperature. Considering the relatively low bandgap of InGaAs (Indium 53%), this is at the same order as the reported InGaAs transistor using a gate last process and ALD High-k dielectric [2].

Conclusion

The $In_{0.53}Ga_{0.47}As$ channel n-channel MOEFET is successfully demonstrated with HfAlO as gate dielectric and TaN as metal gate for the first time using a self-aligned process. XPS shows that for HfAlO as gate dielectric, InGaAs is more effective to suppress the GaO and AsO formation than GaAs. Low gate leakage is observed in the gate stack. Activation temperature of 600 ^{o}C is possible, which is beneficial for high-k gate dielectric integration. I_d-V_d and I_d-V_g characteristics show excellent enhancement mode operation.

Reference

[1] I. Ok, *et al.*, IEDM, Tech. Dig., pp829, 2006.

[2] Y. Xuan, *et al.*, IEDM, Tech. Dig., pp637, 2007.

[3] Y. Xuan, *et al.*, IEEE EDL 28 (11), pp207, 2007.

[4] H.-C. Chin, *et al.*, SSDM, Tech. Dig., pp1050, 2007.

[5] H. J. Oh, *et al.*, Unpublished.

- MBE grown of $In_{0.53}Ga_{0.47}As$
- HCl and $(NH_4)_2S$ surface treatment
- HfAlO deposition
- *In-situ* PDA 500°C 30s
- Sputter TaN deposition
- Gate etch and HfAlO etching
- Si implantation (50KeV/1x$10^{14}$$cm^{-2}$)
- S/D activation @ RTA 600 °C 60s
- S/D and backside contacts fabrication
- Forming gas annealing @ 400 °C 60s

Fig. 1. Process flow of fabricating InGaAs n-channel MOSFET.

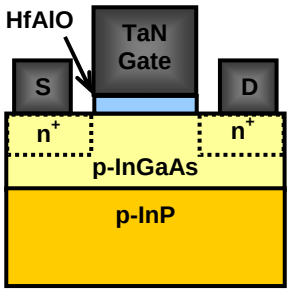

Fig. 2. Schematic of InGaAs n-channel MOSFET with HfAlO.

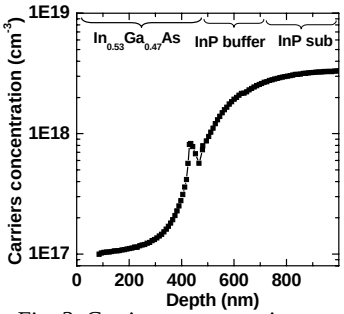

Fig. 3. Carriers concentration versus depth extracted by ECV.

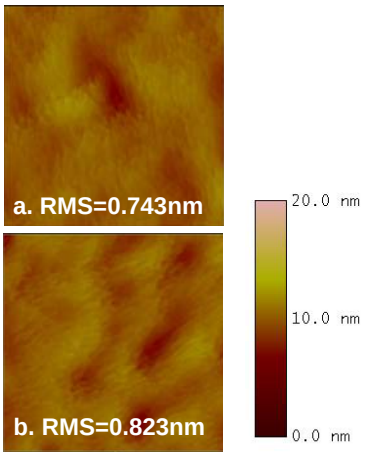

Fig. 4. AFM images of InGaAs (5x5 μm^2) (a) before and (b) after HCl cleaning and $(NH_4)_2S$ treatment.

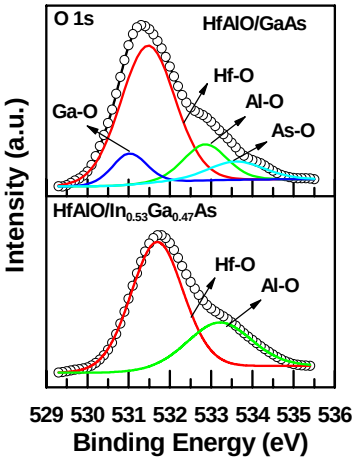

Fig. 5. XPS study of O 1s spectra of thin HfAlO films deposited on GaAs and on InGaAs

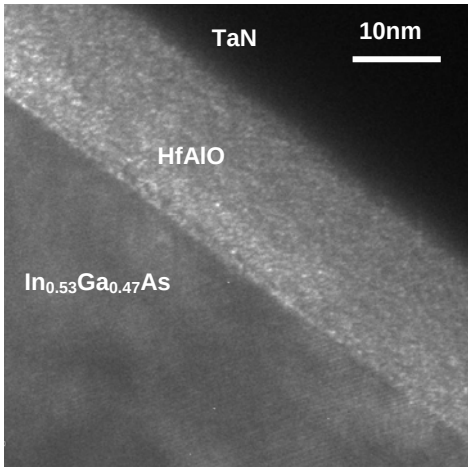

Fig. 6. HRTEM cross sectional image of the stack of TaN / HfAlO/ InGaAs gate stack.

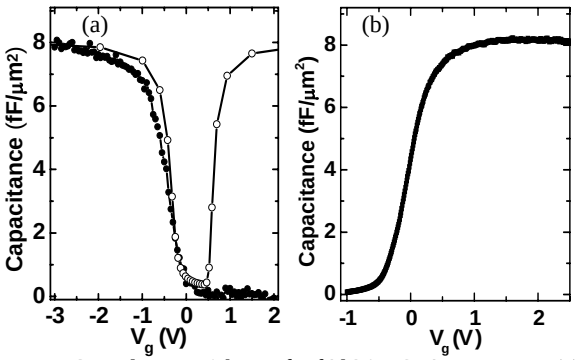

Fig. 7. C-V plots at 10 kHz of HfAlO/ InGaAs transistor (a) at accumulation area measured between gate and substrate with simulated curve fitting (b) at inversion area measured between gate and source combined with drain.

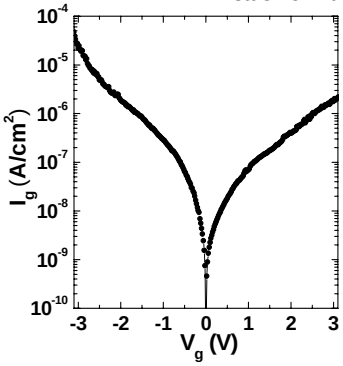

Fig. 8. Gate leakage current for TaN/ HfAlO/ InGaAs gate stack.

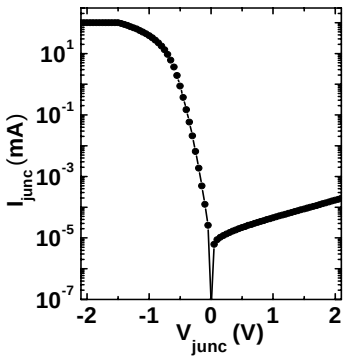

Fig. 9. Excellent rectifying diode characteristic in the Si-implanted InGaAs n^+/p junction.

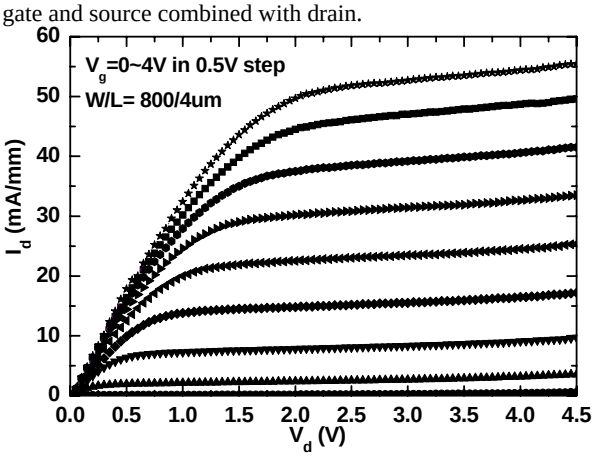

Fig. 10. I_d-V_d characteristic of InGaAs n-MOSFET with a gate length of 4 μm.

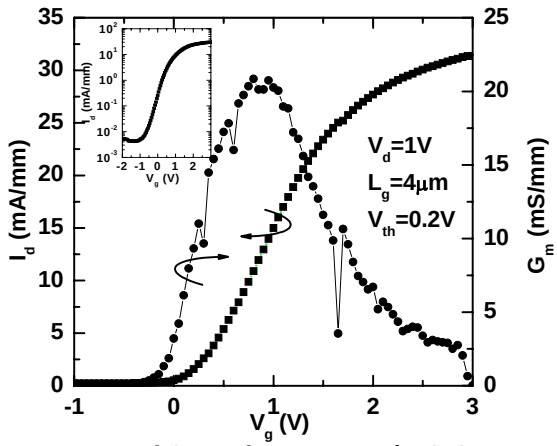

Fig. 11. I_d-V_g and G_m-V_g characteristics of InGaAs n-MOSFET at V_d=1 V; inset showing log scale plot of I_d-V_g.