Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 32-33

B-1-3

High Mobility sub-60nm Gate Length Germanium-On-Insulator Channel pMOSFETs with Metal Source/Drain and TaN MIPS Gate

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Abstract

High mobility (310 cm^2/Vs) and sub-60nm gate length Ge-On-Insulator (GOI) channel pMOSFET is successfully demonstrated for the first time by employing TEOS/SiN stacked gate oxides and NiGe Metal Source/Drain (MSD) to GOI substrates fabricated by the Ge condensation technique. The improved V_{th} roll-off characteristics are achieved down to 60 nm gate length by using GOI structure with back gate control. We have confirmed the device operation of GOI pMOSFETs with gate length of 26 nm. Also, the impact of the Ge concentration and the strain in SiGe-On- Insulator (SGOI) and GOI substrates on the hole mobility in MOS channels is systematically studied for further improvement of MOS current drive. The maximum hole mobility has been obtained near the Ge concentration of 89 % and the compressive channel strain of 1.02 %.

Introduction

A Ge channel has recently stirred a strong interest as a promising candidate for equivalent scaling of CMOS because of its high mobility and high compatibility with present Si CMOS platform. On the other hand, low solubility and high diffusion constant of dopants in Ge make it difficult to fabricate the aggressively-scaled MOSFETs with low source/drain extension resistance. In order to overcome this problem, we have proposed and realized Ge MOSFETs with MSD [1-4]. Recently, we have demonstrated the operation of 60 nm gate length bulk Ge pMOSFETs with MSD [5]. However, the combination with GOI structures is strongly needed for suppressing the short channel effects and the high off-current associated with the small bandgap of Ge and lower potential barrier of MSD. The operation of 110 nm gate length GOI pMOSFETs, using GOI substrates by the Smart-Cut process and ion-implanted source/drain, has been reported very recently [6]. In addition, the introduction of strain is quite important for Ge MOSFETs, in order to obtain much higher current drive than uniaxial compressive strain Si pMOSFETs.

In this study, we successfully demonstrate the operation of MSD SGOI and GOI MOSFETs with gate length of 60 nm or less, for the first time, by using GOI substrates fabricated by the Ge condensation technique [7]. Furthermore, the effect of strain on hole mobility of GOI/SGOI pMOSFETs is studied. The Ge condensation technique can introduce compressive strain, depending on the Ge content, into the SGOI substrates. The SGOI/GOI substrates allow us to systematically study the impact of the Ge content and the strain on the hole mobility in MOS channels. It is found, as a result, that the optimum Ge content exists in terms of the hole mobility enhancement.

Device fabrication

The device fabrication flow is shown in Fig. 1. After formation of SGOI and GOI substrates by the Ge condensation technique, mesa isolation was carried out to define the active area. 10nm SiN was deposited as the gate oxide by hot-wire CVD at a low temperature (under 400°C). 20nm-thick TaN and 10nm thick amorphous Si were sputtered as the gate electrode. The gate patterning was done by E-beam lithography processes with a SiO_2 hard mask. After the gate formation, silicidation of the source/drain and the gate were performed simultaneously, resulting in successful formation of the self-aligned MSD and the silicided poly/TaN MIPS structures. Fig. 2 show the XTEM micrographs of a fabricated 60nm gate length metal S/D pMOSFET with a SGOI (Ge = 89%) channel. The self-aligned smooth MSD junction was clearly observed.

Device characteristics

Characterization of GOI channel metal S/D MOSFET

Fig. 3 shows the I_d-V_g characteristics of a GOI channel metal S/D MOSFET. By applying the back bias, sub-threshold characteristics are improved and, as a result, I_{on}/I_{off} ratio higher than 10^4 can be achieved. Fig. 4 shows the V_{th} roll-off characteristics of a GOI channel pMOSFET and a control bulk Ge pMOSFET. The GOI structure with back bias exhibits better roll-off characteristics down to 60nm. It is also found that the GOI MOSFET with back gate bias exhibits the improved sub-threshold characteristics in comparison with the bulk device, indicating better immunity against short-channel effects in GOI MOSFETs. The I_d-V_g characteristics of a 60nm-gate GOI channel pMOSFET is shown in Fig. 5 with those of a bulk Ge MOSFET for comparison. This is the first demonstration of GOI MOSFETs with gate length less than 100 nm. Furthermore, the FET operation has been observed down to 26nm gate length as shown in Fig. 6. This is the shortest gate length that has been reported so far in Ge channel FETs. These results strongly suggest that GOI MOSFETs are scalable down to 32 nm technology node and beyond. Fig. 7 shows the surface carrier concentration dependence of the effective mobility of the GOI pMOSFET with different SiN thickness and the bulk Ge pMOSFET. It is found that x3 higher hole mobility against the Si universal one can be achieved by optimizing the gate stack structure (TEOS:6nm /SiN:0.8nm) and improving the interface properties.

Ge concentration and strain dependence of hole mobility of SGOI channel pMOSFETs

Five types of substrates with different values of the Ge concentration and the strain, shown in Table 1, were prepared by the Ge condensation technique, which can control the Ge concentration and thickness of SGOI substrates, in order to find the optimum Ge content in terms of the mobility. A TEM micrograph of a typical SGOI wafer is shown in Fig. 8. The channel thickness and the strain in the substrates were measured by TEM and NBD, respectively. It is found that the compressive strain is gradually relaxed with increasing the Ge concentration and that the strain is completely relaxed in pure GOI. Fig. 9 shows the I_d-V_g characteristics of the SGOI channel pMOSFETs with different Ge concentrations. The effective mobility with the different Ge concentration is shown in Fig. 10. It is found that the mobility increases with increasing the Ge concentration and exhibits a peak (x2 higher than the Si universal hole mobility) at x of 89%, which has 1.02% compressive strain. In the Ge content with x of 95% and 100%, however, the mobility decreases, attributed to the strain reduction. It is confirmed that GOI substrates, i.e., with x of 100%, yield almost the same hole mobility as in the Ge bulk MOSFETs. These results mean that there the optimum Ge content from the viewpoint of the mobility enhancement can exist, because of the Ge content dependence of strain, which is another important factor for further improving the performance of Ge MOSFETs.

Conclusions

We have successfully demonstrated the high mobility metal S/D GOI p-MOSFETs with silicided poly/TaN MIPS gate on GOI substrates fabricated by the Ge condensation technique. We have confirmed the operation of GOI p-MOSFETs with gate length of 26 nm. The high hole mobility (310 cm^2/Vs) and the successful operation of sub-60nm gate length GOI channel pMOSFET has been achieved, for the first time, by using TEOS/SiN gate stacks. Also, the Ge content of hole mobility in GOI/SGOI pMOSFETs using the Ge condensation substrates has been studied. It has been found that high Ge content and compressive strain SGOI channels can provided the maximum hole mobility.

Acknowledgement
The authors would like to thank Drs. M. Hirose, T. Kanayama and T. Masuhara for their continuous supports. This work was supported by NEDO.

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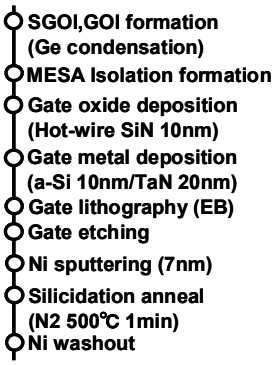

Fig. 1. Process flow used in this work.

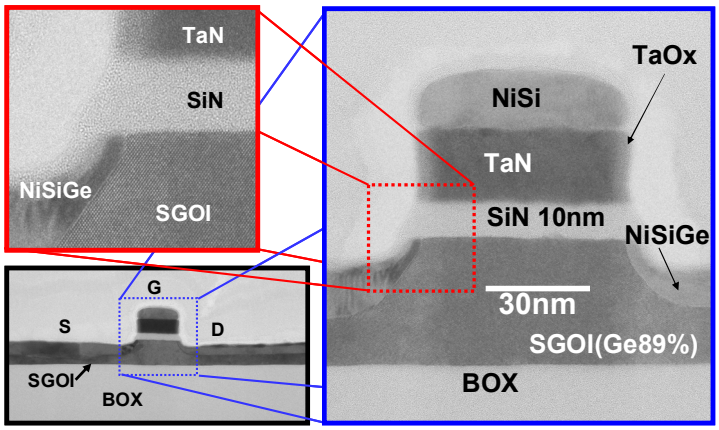

Fig. 2. XTEM micrograph of a 60nm gate SGOI (Ge = 89%) channel metal S/D pMOSFET.

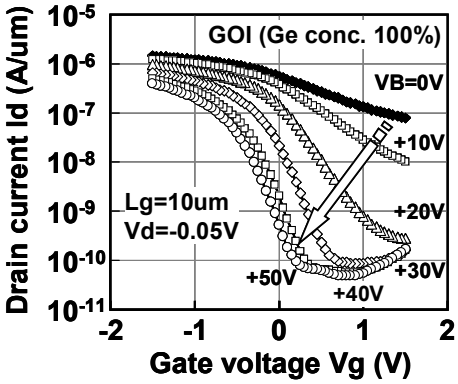

Fig. 3. Id-Vg characteristics of GOI channel pMOSFET with different VB. Poor Subthreshold behavior caused by residual p-doping effect and poor Ge/BOX interface properties were suppressed by body bias.

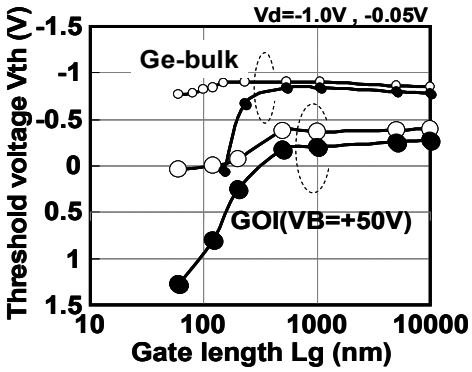

Fig. 4. Vth roll-off characteristics of GOI channel pMOSFET to comparison with bulk Ge pMOSFET. Improved roll-off characteristics were achieved by GOI structure and body bias effect.

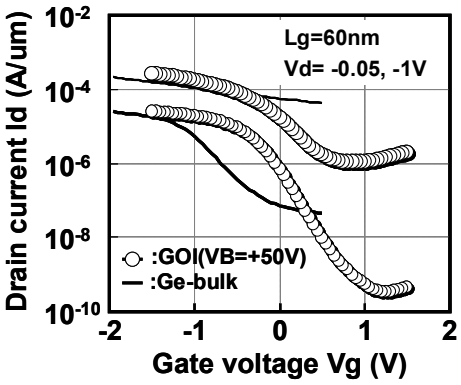

Fig. 5. Id-Vg characteristics of 60nm-gate GOI channel pMOSFET. The GOI MOSFET with back gate bias exhibits the improved sub-threshold characteristics in comparison with the bulk device.

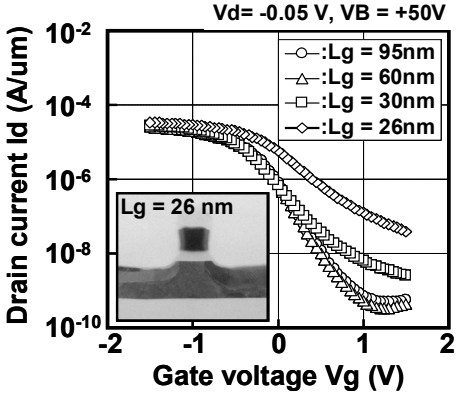

Fig. 6. Id-Vg characteristics GOI channel pMOSFETs. The FET operation was observed down to 26nm gate length. This is the shortest gate length Ge channel FET which is reported so far.

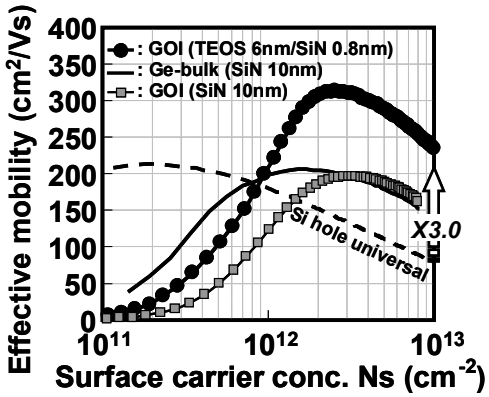

Fig. 7. Surface carrier concentration dependence of effective mobility of GOI channel pMOSFET to comparison with bulk Ge pMOSFET. By optimizing the gate oxide structure, X3 times higher hole mobility was achieved compared with Si hole universal.

	Ge con.(%)	T_{SGOI} (nm)	Strain (%)
SGOI	78	44	-1.444
SGOI	86	41	-1.360
SGOI	89	36	-1.024
SGOI	95	35	-0.993
GOI	100	31	0

Table 1. Summary table of SGOI,GOI wafer splits. T_{SGOI} and Strain were determined by TEM and NBD, respectively.

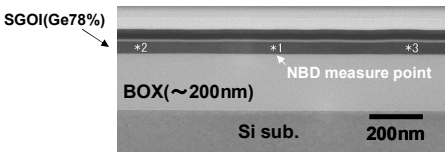

Fig. 8. XTEM micrograph of typical SGOI wafer.

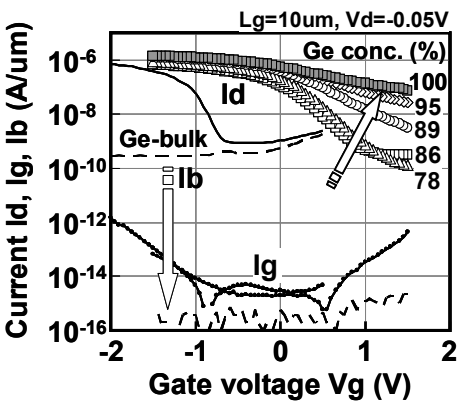

Fig. 9. Id-Vg characteristics of SGOI channel pMOSFETs with different Ge concentrations. Ioff were monotonically increased with increasing Ge concentration even though suppressed Ib.

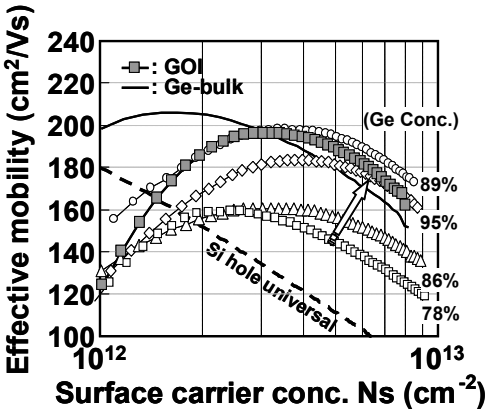

Fig. 10. Surface carrier concentration dependence of effective mobility of SGOI channel pMOSFETs with different Ge concentrations.