Accuracy Assessment of Charge-Based Capacitance Measurement for Nanoscale MOSFET Devices

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Abstract – Charge-Based Capacitance Measurement (CBCM) techniques are promising not only for small size interconnects [1] but also for small capacitance of active devices [2].[3]. In this paper, the factors that decide the lower limits of measurements as well as the sources of errors are evaluated based on extensive mixed device and circuit mode simulations. The role of the parasitic capacitance of the source/drain terminals of the devices constituting the pseudo-inverter is clearly delineated.

INTRODUCTION Accurate measurement of ultra-small capacitance is crucial to successful device characterization and development of compact models for circuit applications of the next-generation nanoscale devices. Direct AC small signal measurements is extremely challenging when capacitance of device under test (DUT) falls below tens of femto-farads [4]. CBCM technique, originally proposed by Chen *et al.* for passive interconnect capacitance measurement [1], has recently been used for characterizing the non-linear gate capacitance of MOS devices [2][3]. As shown in Fig. 1, the capacitance C_{DUT} is given by the difference in the average current between the test branch loaded with DUT, I_{Vdd} , and the current in the reference branch, I'_{Vdd} .

$$I_{Vdd} - I'_{vu} = C_{DUT} \cdot V_{dd} \cdot f \tag{1}$$

For voltage dependent capacitance, C_{DUT} equivalent to small signal capacitance, is obtained by differentiation:

$$C_{DUT} = \frac{d(Q_{VAd} - Q_{VAd})}{dV_{V}} = \frac{d(I_{VAd} - I_{VAd})}{dV_{V}} \frac{1}{f}$$
(2)

where f is the frequency of non-overlapping signals to the gates of the pseudo-inverter driver devices [Fig. 1(a)]. Turning the drivers on and off alternatively by non-overlapping pulses charges and discharges the DUT and the parasitic capacitance between ground and V_{dd} [Fig. 1 (d)]. The main source of error in the measurement is the charge injection through C_{gs} of PMOS driver during its switching-off process. The amount of charge injected to V_{dd} depends on the rise/fall times of the pulses, magnitude of C_{ed} and on the load to the pseudo-inverter. Further, in case of low capacitance of the DUT, the currents in the two branches can be of similar order giving rise to loss of accuracy during the subtraction and differentiation process. Any difference in charge injection in the reference branch and the DUT branch may have magnified impact on accuracy in case of small capacitances. The charge injection issue has been addressed in two ways: (i) by using the pseudo inverters consisting of pass-gates instead of single transistors as shown in Fig. 1 (b) [5] and (ii) by measuring the reference and DUT currents on the same pair of pseudo-inverters [3]. In the second technique, the DUT is proposed to remain uncharged during the measurement of the reference current by precharging the DUT to V_{DD} level by a third pulse at the Source and Drain (S&D) of DUT as in Fig. 1 (c)-(d). To assess the efficacy of these techniques, TCAD simulations provide the best tool for evaluation as the instantaneous voltages on the nodes and currents in branches and electrostatics and carrier dynamics inside the device structure can be easily tapped.

SIMULATION SETUP Mix-mode simulations in MEDICI were used to simulate the CBCM technique. The DUT chosen is gateall-around nanowire device that has a gate length of 0.25µm and cylindrical diameter of 10nm. 'WIDTH' parameter was used in MEDICI as the multiplicity parameter to simulate multiple "fingers" of DUT connected in parallel. The main advantage of using a physical DUT in place of a compact model used in [5] is that physical DUT will automatically account for all the physics of charge movement including non-quasi-static effect, if any. On the other hand, N and PMOS drivers that essentially function as switches with attached junction and overlap capacitances can be well emulated by compact models. For all compact model drivers, we have gate length of 0.18µm and width of 0.5µm. This setup, thus, captures the nanoscale DUT physically, ensures proper convergence and economizes on computational resources. Repetition rate of 45 MHz, higher than that used in [2] and [5] was chosen in this study for two reasons: (i) more pronounced charge injection problem at higher frequency allows meaningful evaluation of the different methods; and (ii) higher frequency gives higher I_{Vdd} , which would allow better accuracy during measurements Also, our simulations indicated insignificant effect of the frequency of input pulses on the extracted C-V characteristics of the DUT.

RESULTS AND DISCUSSION

A. Charge injection Shown in Fig. 2 are the input pulses and the voltage tapped at the common drain of pseudo-inverter [labeled X in Fig. 1 (a)- (c)]when V_{dd} is 0.8V. For setup in Fig. 1(a), both V_{REF} and V_{DUT} shoot up significantly beyond V_{dd} during the turning-off of the PMOS, indicating a higher charge injection. As for the set up in Fig. 1(c), the voltage overshoot of V_{DUT} is lower compared with V_{DUT} of 1(a) case (which is equivalent to the case when a constant voltage is applied to DUT in Fig. 1 (a)). Also worth noticing is the difference of the voltage levels for the two setups depicted in Fig. 1 (a) and (c) - although the difference is less in the latter, it has not been fully eliminated. More interesting is the case of setup in Fig. 1 (b) shows a little "undershoot" below V_{dd} indicating a charge injection in the reverse direction, which is ascribed to the mismatch in the parasitic capacitors and V_{dh} of the two transistors comprising the pass gate.

B. Measurement accuracy The bias-dependent capacitances of DUTs with various number of fingers derived using the three CBCM methods are shown in Figs. 3-5. All three methods are accurate for 100 finger DUTs. However, when the DUT capacitances become comparable to or lower than the parasitic capacitance of the pseudo inverters, the effect of charge injection becomes more obvious and the derived capacitance becomes less accurate in all the cases. This is further quantified in Fig 6. The setup in Fig. 1 (b) with pass-gates to reduce impact of charge injection suffers the least inaccuracy. In this particular case, the RMS error is less than 2.2% even with a 3 finger DUT (which represents a total DUT capacitance of ~1.35fF). The setup in Fig. 1(c) is accurate for large capacitance with the accuracy degrading for smaller capacitances. In actual measurements, the average current, magnitude of which is proportional to the frequency of input pulses, and pulse repetition period give the charge. The measurement accuracy is typically specified as a fraction of the measured value. To emulate the effect of measurement accuracy, we introduced a random noise of different magnitudes up to 1% in the integrated charge. In Fig. 7, the RMS error is plotted against the maximum % of the introduced random noise. It shows that in order to measure the low values of capacitance accurately, the average currents in the CBCM methods should be measured to 0.1% accuracy or better. This requirement would progressively relax for relatively higher values of DUT capacitance.

C. Role of parasitic capacitance In three CBCM setups, the extracted DUT capacitances are referenced to the parasitic capacitance of pseudo inverter at the drain junction. Therefore inaccuracy in either capacitance can be amplified in C_{DUT} by the subsequent subtraction. The parasitic capacitances for the three CBCM setups, along with the analytical calculation from HSPICE compact model are plotted against V_{dd} in Fig. 8 (a)-(c). The differences between the two are mainly due to charge injection and numerical differentiation (noise). In Fig. 8 (b), the level of noise and the parasitic capacitance shows a clear dependence in C_{DUT} . But in case of 8 (b), the noise is consistently reduced for all size of DUT capacitances. This explains the better accuracy of the Fig. 1 (b) setup in capacitance measurement as shown in Fig. 5.

CONCLUSION In this paper we have reported for the first time the detailed evaluation of different variants of the CBCM technique reported in the literature. We find that pseudo-inverters comprising the pass-gates take care of the charge injection in a best possible way. Also, the current needs to be measured with an accuracy better than 0.1% for accurate measurement of smaller capacitances (<1fF).

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Fig.1: CBCM test keys (a): proposed by Chen et al.[1] for interconnect capacitance (b): proposed by Vendrame et al [5]. Charge feed back in N- and Ptransistors of the pass gates is expected to 'balances' out (c) proposed by Chang et al[3]. It relaxes the demand on 'matching' as same drivers are used two times. (d): Input pulses I - at P driver gate. II – at N driver gate. III – at S&D of DUT in setup (c). Dashed line in III indicates the constant voltage applied to S&D to scan the V_{gs} for both polarities.



Fig 2: (a) Input and simulated output voltage wave forms for the three methods. For setups of Fig.1(a) and 1(b), V_{DUT} is at the gate of DUT and V_{REF} is tapped at X in the reference branch. V_{dd} is 0.8V. Setup in Fig. 1(b) reduces overall amount of charge injected. Setup of Fig.1 (c) reduces difference in charge injection for two measurements when PMOS is switching off. The imbalance during the falling and rising edges of the pulse at S/D may not be significant as P-driver is off. (b): The current waveform in the reference and the DUT branch for the setup shown in Fig. 1 (a). The rising/falling edges of Fig.2(a) are identified by arrows. Inset zooms in the charge injection current during the rising edge of PMOS gate pulse in the reference and the DUT branches.



Fig 3: Bias-dependent capacitance derived by CBCM setup of Fig 1 (a). DUTs with 1, 10, and 100 parallel fingers are considered and compared with the exact capacitance (small signal AC analysis in MEDICI). The error is very large for one finger DUT (max capacitance ~0.45fF).



Fig. 4: Bias-dependent capacitance derived by the CBCM setup in Fig. 1 (b) with 5, 10, and 100 parallel DUT fingers. Solid line is the exact capacitance calculated by AC small signal method in MEDICI. This method is accurate even at 3 finger DUT (Max cap=1.35fF).



Fig. 5: Bias-dependent capacitance derived by the CBCM setup in Fig. 1 (c) with 3, 5, and 100 parallel DUT fingers. Solid line is the exact capacitance calculated by AC small signal method in MEDICI. Large errors are observed for DUTs with 5 or lesser no. of fingers.



Fig. 6: RMS error plotted against number of DUT fingers for the three methods. Accuracy for setup of Fig. 1(b) is not much degraded even for small DUT capacitance (1.35fF). Setups of Fig. 1(a) and 1(c) show larger RMS error for smaller capacitances.



Fig. 7: RMS error plotted against introduced random error in the charge for setups of Fig. 1(a)-(c). Large DUT capacitance enhances tolerance to error in all the methods.



Fig. 8: Effective parasitic capacitance extracted from reference branch (a): setup of Fig. 1(a) (b): Setup of fig. 1(b) and (c): Setup of Fig. 1(c). Solid lines are the capacitance from the compact model. The differences in magnitude are due to charge injection and noise is mainly contributed by numerical differentiation.