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Impacts of Random Dopant Fluctuation on Transient Characteristics in CMOS Inverters: A Device Simulation Study

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***Abstract*- Intrinsic gate delay variations in CMOS inverters due to random dopants are studied by using in-house classical drift-diffusion device simulator. We demonstrate for the first time that the intrinsic delays of ultra-small inverters innately show asymmetrical distributions, defined by the carrier saturation velocity. Also, we explain the correlation between the delays and the through currents, comparing the surface potentials between the fastest and slowest transition cases.**

1. Introduction

It is widely recognized that random dopant fluctuation (RDF) effects cause variations in the device characteristics. The effects in individual devices have been intensively studied by using device-level simulator [1] [2], yet, as for the variation analysis beyond individual devices, circuit-level simulator with analytical variation models still plays a major role [3]. However, since it is not an easy job to estimate equivalent circuits for decanano MOSFETs, device-level simulator analysis, being free from those tasks, has potential advantages. Except for its high computational costs, device-level simulator enables us to understand the characteristics of small circuit without the knowledge of equivalent circuits. Actually, Tanabe et. al. studied static noise margin (SNM) variations in 6-Tr. SRAMs all by device simulator [4]. But their interest was concentrated on the SNM, not referring to the dynamical property variations. In this study, we investigate the intrinsic gate delay variations due to RDF in 20-nm CMOS inverters, using our in-house classical 3D drift-diffusion (DD) simulator [5]. The objective of this study comprises two parts: one is to exhibit an application example of device-level simulator analysis for computing transient characteristics of small circuit in the decanano regime; and the other is to qualitatively point out the physical reason controlling the delay variations by regarding RDF as the only noise source. Therefore, the other noise factors, such as supply voltage fluctuation [6], are ignored.

2. Simulation and discussion

In this time, our device simulation is based on the classical DD approach. We separate the Coulomb potential of individual impurities into the short- and the long-range components [2], and only the latter components are incorporated into our Poisson solver, in order to avoid the double counting of the former components already included in the mobility model. In fact, the present scheme is validated by recent Monte Carlo simulations in which this separation gives the exact Coulomb-limited mobility [7].

Figure 1 shows the CMOS inverter structure we used in this study. It should be noticed that, to consider ideal situation for integration, both n^+- and p^+- polysilicon gates are assumed to have the same width. Instead, in order to adjust driveability of p- and n-MOSFETs, in this case, we use the same low-field mobility for electron and hole. The transient responses of the inverter to a square wave input for 75 different impurity profiles are shown in Fig. 2. The overshoot-like outputs exceeding the input voltage range are derived from the p-n junction capacitance between the common drain and channels. Histograms of the falling delay (*tdhl*) and the rising delay (*tdlh*) are summarized in Fig. 3. The delays in this study are defined as the time required for V_{out} to reach $V_{\mathrm{dd}}/2$ level. It is understood that both distributions in Fig.3 have positive skew. The transient response is governed by the following differential equation,

$$C_{load}\frac{dV_{out}}{dt} = \mp I_d(V_{in}, V_{out}),$$

where –/+ signs correspond to the falling and the rising case, respectively. I_{d} of the rhs varies between the pentode and the triode characteristics depending on V_{out}, but the domain is apparently $0 \le I_{\mathrm{d}} \le I_{\mathrm{d,max}}$, where $I_{\mathrm{d,max}}$ is limited by the maximum carrier velocity attainable in the channel. Thus, integrating both sides of the above equation until V_{out} reaches $V_{\mathrm{dd}}/2$, we obtain a simple expression for possible delay range: $C_{\mathrm{load}}V_{\mathrm{dd}}/(2I_{\mathrm{d,max}}) \le \tau < \infty$. As the gate length is scaled down, the stronger transverse electric field easily saturates carrier speeds. Hence, the delays in ultra-small inverters tend to skew toward the slower direction.

Next, in order to examine the relation between RDF and the falling delay, the impurity atom distribution near the surface of p- and n-MOSFETs are plotted for the slowest (Fig. 4) and the fastest case (Fig. 5). In the falling transition, n-MOSFETs take on the driving transistor. Since the macroscopic concentration of channel impurity is set to be 2.5×10^{18} cm^{-3} (Fig. 1), about 8 impurity atoms are expected to be found in the $20 \times 20 \times 8$ nm^3 volumes under the gate electrode. However, it is clearly seen that, while as many as 16 acceptors are contained in the slowest case, as only as 5 acceptors are contained in the fastest case. These differences apparently cause channel resistance variation, or equivalently, the variations of surface potential height (Fig. 6). Same mechanism holds for the rising transition in the p-MOSFETs. Figure 7 shows scatter plots between the gate delays and the through currents. It certainly indicates a correlation; the higher through currents, the shorter intrinsic delays. From these figures, it is found that RDF near the channel surface produces the high/low p-n junction barrier variations, resulting in the slow/fast delay variations.

3. Conclusion

In summary, intrinsic gate delay fluctuations due to RDF in 20-nm CMOS inverters were studied using 3D DD simulator. It is found that the high/low surface potential variations caused by RDF in the driver transistor introduce through current variations, resulting in intrinsic switching speed variations. The intrinsic gate delay distributions skew toward the slower direction, reflecting the physical limit of the maximum carrier velocity achievable in Si channel.

References

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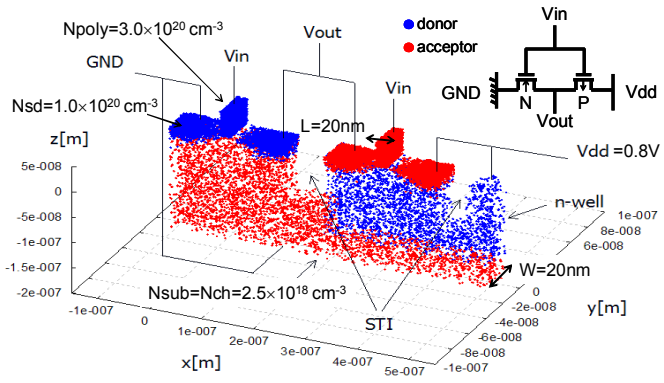

Fig.1 : Schematic view of the simulated CMOS inverter structure

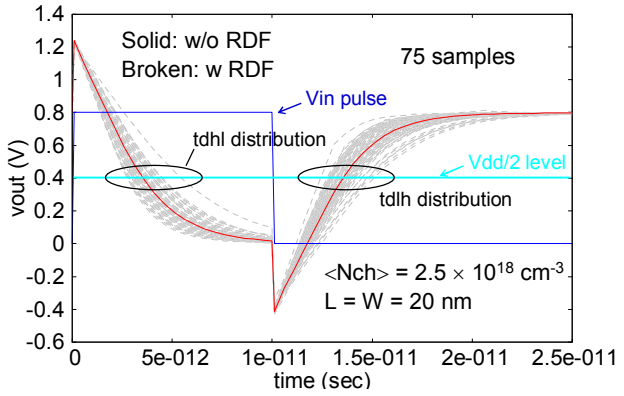

Fig.2: Transient responses of 20-nm CMOS inverters

$$\int_0^{tdhl} dt = \int_{V_{dd}}^{V_{dd}/2} -\frac{C_{load} dV_{out}}{I_d(V_{in}, V_{out})}, \quad 0 \le I_d \le I_{d\max} \rightarrow \quad \frac{C_{load} V_{dd}}{2 I_{d\max}} \le tdhl < \infty$$

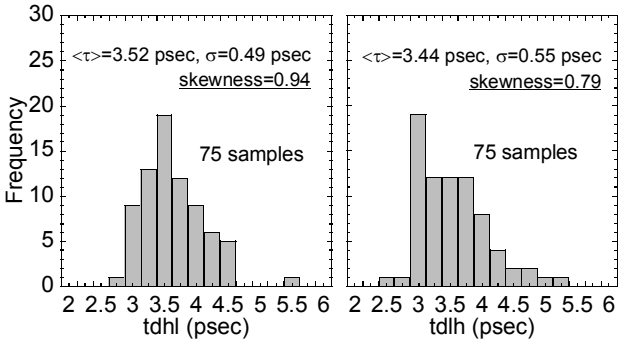

Fig.3: Histograms of the intrinsic falling delay (left) and the rising delay (right).

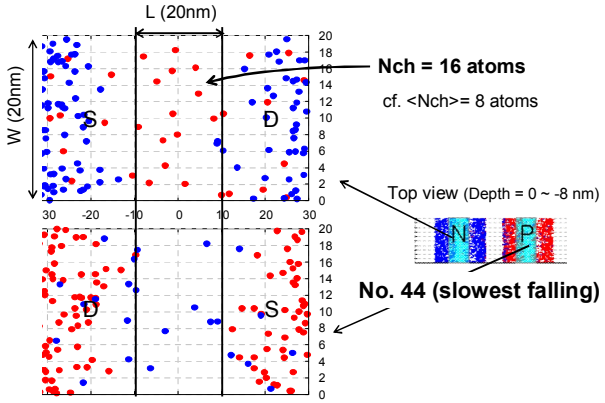

Fig.4: Impurity profile near the surface in the slowest falling case

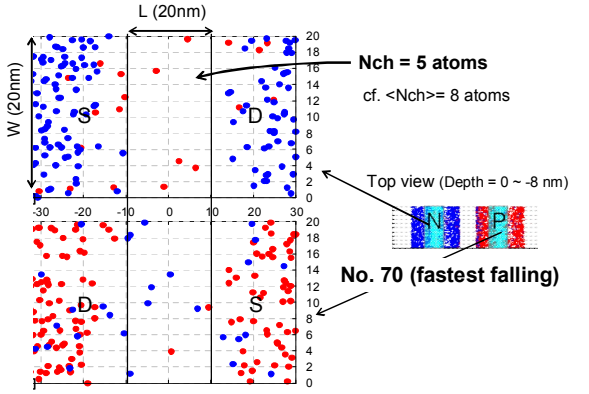

Fig.5: Impurity profile near the surface in the fastest falling case

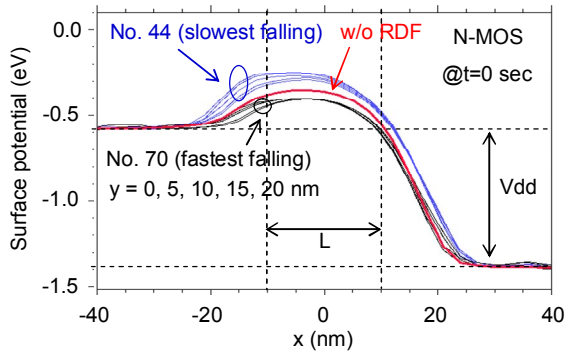

Fig. 6: Surface potentials of n-MOSFETs along the channel

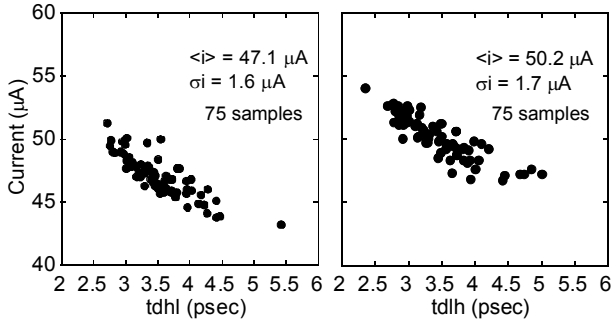

Fig. 7: Correlations between through currents and transient delays