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Discrete Dopant Fluctuated Transient Behavior in 16-nm-Gate CMOS

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1. Introduction

Various random dopant effects have recently been studied for nano-CMOS fluctuation in both experimental and theoretical approaches [1-3], but attention is seldom drawn to the existence of transient behavior fluctuations of active device due to random dopant placement. In this study, the device's gate capacitance fluctuations and signal propagation variation of the 16-nm-gate CMOS inverter circuit are explored by 3D "atomistic" device-circuit coupled mixed-mode simulation technique which concurrently captures "dopant concentration variation" and "dopant position fluctuation". Two fluctuation suppression techniques, shunted NMOS device and doping profile improvement, have been implemented to suppress the associated intrinsic fluctuation. The result of this study provides insight into the random-dopant-induced device's gate capacitance and timing characteristic fluctuations in nano-CMOS.

2. Methodology and Results

All statistically generated discrete dopants, shown in Fig. 1, are incorporated into the large-scale 3D device simulation under parallel computing system [4]. The simulation is performed by solving a set of 3D density-gradient equation coupling with Poisson equation as well as electron-hole current continuity equations. Figures 1(a)-1(d) show the 758 discrete dopants randomly distributed in the 80 nm^3 cube with an average concentration of $1.48 \times 10^{18} cm^{-3}$. The 80 nm^3 cube are then partitioned into 125 sub-cubes of 16 nm^3, where the dopants may vary from zero to 14 (the average number = six) within its sub-cubes. These sub-cubes are then equivalently mapped into the 3D device channel region, as shown in Fig. 1(e). A CMOS inverter, as shown in Fig. 1(f), is used as test circuit for studying the transient behavior of circuit, where both the channel doping of the NMOS and PMOS FETs are treated discretely. To obtain physically sound result, 3D device-circuit coupled mixed-mode simulation with discrete dopants is employed to examine the transient behavior of circuit. We notice that the developed large scale simulation methodology and the physical models of the examined devices have been experimentally validated [2] for the best accuracy.

Figure 2 shows the spreading ranges of C-V characteristics for the 125 discrete dopant fluctuated 16-nm-gate planar MOSFETs. The shift and variation of C-V curves are observed. The total gate capacitance ($C_{g,total}$) is summation of the gate-drain capacitance (C_{gd}), the gate-source capacitance (C_{gs}), and the gate-bulk capacitance (C_{gb}). For the $C_{g,total}$ fluctuation, as shown in Fig. 2(a), the maximum fluctuation of $C_{g,total}$ is reduced as the drain voltage is increased. The wider of depletion layer at the drain junction decreases the C_{gd} and thus exhibits less fluctuation, as shown in Fig. 2(b). Moreover, the position of the maximum fluctuation of $C_{g,total}$ is shift due to the increase of drain bias. For the fluctuation of C_{gs}, because of the channel length modulation at drain voltage of 1 V, the charges are accumulated near the source junction. The C_{gs} and its fluctuation are increased, as shown in Fig. 2(c). As for the fluctuation of C_{gb}, as shown in Figs. 2(d) and 3(d), due to the relatively larger distance between gate and substrate, the contribution of C_{gb} and its fluctuation to $C_{g,total}$ is insignificant. The fluctuation of the gate capacitance is crucial for circuit transient behavior. Figure 3(a) shows the input/output signals for the discrete dopant fluctuated CMOS inverter, where the fall and rise characteristics are zoomed-in, as shown in Figs. 3(b) and 3(c). The fluctuations of rise time and fall time are about 0.32 ps and 0.37 ps, respectively. The fall time is the time required for the output voltage varying from 90% of the logic "1" level to 10% of the logic "0" and the rise time is the time required for the output voltage varying from 10% of the logic "0" level to 90% of the logic "1". Figures 4(a) and 4(b) show the fluctuations of the signal transition points for the fall and rise transitions, respectively, where the definitions of them are given in Figs. 3(b) and 3(c). For the fall transition, the output signal falls as the NMOS is turned on. Therefore, the fluctuation of the signal transition points for the fall time is determined by the threshold voltage of the NMOS transistor, which is fluctuated by random dopants inside channel. Therefore, as the number of dopant in NMOS channel is increased, the fall time signal transition point is delayed, and therefore it induces the delay of circuit. On the other hand, the characteristics of signal transition points for the rise time can be inferred similarly. To investigate the fluctuation suppression in transient behavior, according to circuit design and device technology points of views, an inverter with a shunted NMOS devices and an inverter with improved doping profile are further advanced. Figure 5(a) summarized the rise time and fall time fluctuations for the studied fluctuation suppression techniques. Results show that for the circuit level suppression technique, an inverter with the shunted NMOS devices, exhibits the best results, where the rise time and fall time fluctuations are 23% and 29% smaller than the original inverter. However, the increase of the transistor number in circuit may increases the load capacitance. Therefore, the rise time and fall time are increased 0.04 and 0.2ps, respectively. Also, the area of the circuit is enlarged. As for the inverter with an improved doping profile, the rise time and fall time fluctuations are 16% and 14% smaller than the original inverter, where the load capacitance and circuit area are the same as original.

3. Conclusions

The variation of device gate capacitance and transient behavior of the 16-nm-gate CMOS circuit have been explored. For the studied nano-CMOS inverter, the number of discrete dopants, varying from zero to 14, may result in 5.4% variation of the rise time and 6.2% variation of the fall time. The inverter with shunted NMOS transistors may have the better results than that with doping profile improvement. However, the signal transition time and circuit's area will be increased. To pursue fast signal propagation and avoid the additional area of transistor, the device with doping profile optimization will be an alternative.

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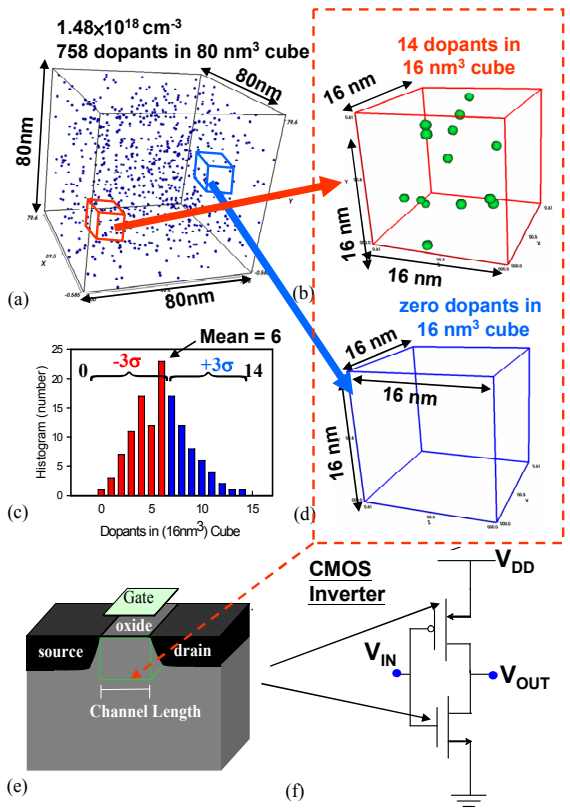

Fig. 1. (a) Discrete dopants randomly distributed in the 80 nm^3 cube with the average concentration of 1.48x10^{18} cm^{-3}. There will be 758 dopants within the cube, but dopants may vary from zero to 14 (the average number is six) within its 125 sub cubes of 16 nm^3, [(b), (c), and (d)]. The 125 sub cubes are equivalently mapped into channel region for dopant position/number-sensitive device simulation as shown in (e). (f) The CMOS inverter as test circuit for timing fluctuation analysis, where the device-circuit coupled mixed-mode simulation is conducted.

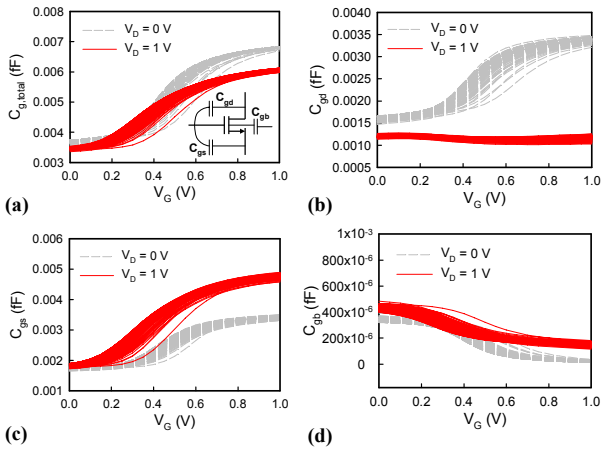

Fig. 2. (a) Total gate capacitance ($C_{g,total}$), (b) gate-drain capacitance (C_{gd}), (c) gate-source capacitance (C_{gs}), (d) and gate-bulk capacitance (C_{gb}) of the 125 discrete dopant fluctuated 16nm-gate planar MOSFETs. The shift and variation of C-V curves are observed. The total gate capacitance is summation of the gate-drain capacitance, the gate-source capacitance, and the gate-bulk capacitance.

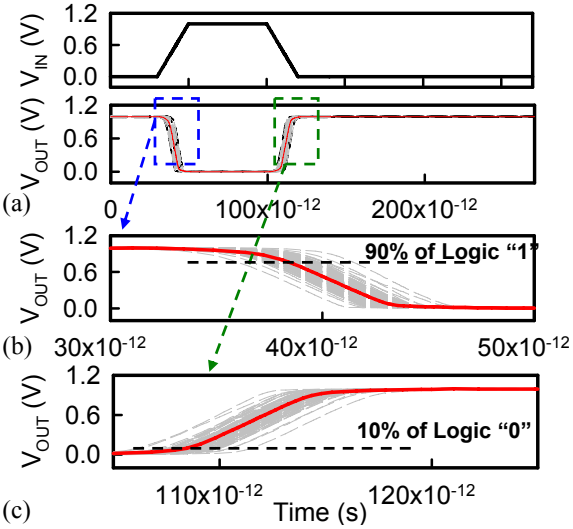

Fig. 3. The (a) input/output signals for the studied discrete dopant fluctuated inverter circuits. The corresponding (b) fall and (c) rise characteristics are plotted in detail.

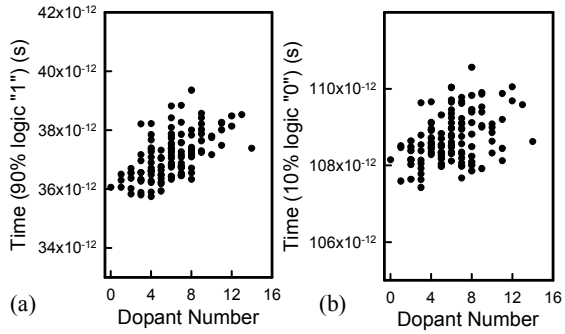

Fig. 4. The fluctuations of (a) fall and (b) rise signal transition points for the discrete dopant fluctuated inverter circuits, in which the transition points are defined in Figs. 3(b) and 3(c)

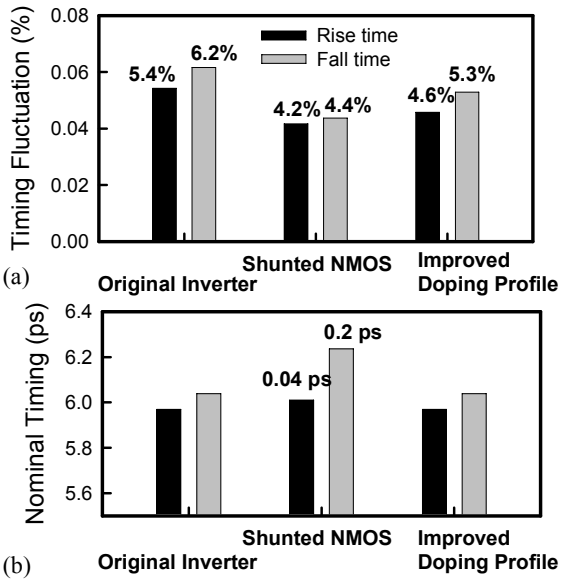

Fig. 5. Comparison of the (a) timing fluctuation, (b) and nominal rise/fall time for the original inverter, a shunted NMOS inverter, and an inverter with improved doping profile.