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Recent Progress in Carbon Nanotube Electronics – Modeling, Materials, Devices, Circuits, and Interconnects

H.-S. Philip Wong

Department of Electrical Engineering and Center for Integrated Systems
Stanford University, Stanford, CA 94305, U.S.A.
Phone: +1-650-725-0982 E-mail: hspwong@stanford.edu

1. Introduction

This year marks the 10th anniversary of the first publication of the carbon nanotube transistor [1, 2]. While there have been significant accomplishments in fundamental understanding and discovery, the engineering work that is required to harness carbon nanotube into useful technologies is just beginning. This paper reviews recent progress in carbon nanotube electronics, focusing on logic applications including the transistor and the interconnect wires.

2. Device Modeling and Design Tools

Device and circuit design and performance estimation require the use of modeling tools with appropriate level of abstraction. A compact model for circuit simulation (SPICE) has been developed (Figs. 1, 2) [3]. The tool is now used by research groups around the world. It captures the essential physics of the band structure, inter-channel screening, and parasitic capacitances of the device structure. Using this compact model, we performed circuit simulations to compare the energy and delay of CNFET with Si CMOS (Fig. 3). Device parameter variations and the presence of metallic CNTs were included. The results highlight two important requirements for the material: (a) a high density of CNT (250 CNT/μm) is required to provide enough current drive; (b) the presence of metallic CNTs substantially degrades the performance [4]. We have also developed analytical models of the density of states and carrier density to aid in physical intuition for device design [5]. A simplified version of the compact model has also been developed to enable system-level optimization [6].

3. Material Synthesis

Full-wafer aligned CNT growth has been achieved by growing on properly annealed quartz substrates [7] (Fig. 4). Using a technique akin to wafer bonding, the CNTs can be first transferred to a handle substrate and subsequently placed onto the target substrate (e.g. SiO_2/Si) [7] (Fig. 5). A typical density of 5 CNT/μm is achieved. This is still significantly below the required target of 250 CNT/μm [4].

4. Transistors and Logic Circuits

Transistors that consist of single CNTs have normalized I-V characteristics that outperform Si CMOS [8]. The first demonstration of AC gain for a CNFET was performed using a common source amplifier [9] (Fig. 6). The frequency response was limited by parasitic capacitance and corroborated the need to have multiple aligned CNTs per device [10]. A step toward VLSI-compatible logic circuit fabrication was made using full-wafer aligned CNT growth and CNT transfer, coupled with full-wafer optical lithography. Mis-positioned-CNT-immune logic structures with multiple CNTs per transistor were demonstrated (Fig. 7) [7]. We built library cells for universal logic structures (NAND, NOR) and more complex structures (AND-OR-INVERT), thereby illustrating the general applicability of the design and fabrication strategy [4, 7]. Key issues remain: complementary n- and p-doping, presence of metallic CNTs, proper threshold voltage (V_t) setting and tuning, device stability.

5. Interconnect Wires

Simulations have shown the potential of CNTs for on-chip interconnects [11]. The theoretically-lower resistance of metallic multi-wall CNT interconnects enables narrower wires with smaller pitches for a given frequency target, thereby yielding die area saving, and hence power saving [12]. Fig. 8 shows a massively parallel test vehicle for gathering statistics of electrical properties of hundreds of CNT wires [13]. Until recently, there has been no experimental demonstration of high-speed ***digital*** signal propagation in metallic CNTs for interconnect applications. Fig. 9 shows a CMOS ring oscillator test platform which integrates CNT wires with Si CMOS, achieving >1GHz digital signal propagation through CNT wires [14].

6. Conclusions

Significant progress has been made in the broad technical community toward developing a carbon-based technology. Many of the performance expectations have yet to be experimentally demonstrated. The use and development of suitable modeling tools will continue to set performance expectations and help identify future development needs.

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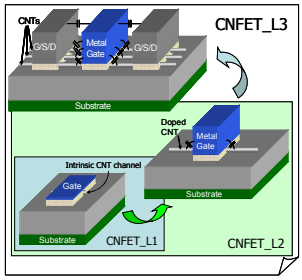

Fig. 1 The complete CNFET device model is implemented hierarchically in three levels [3]. Available at http://nano.stanford.edu/models.php

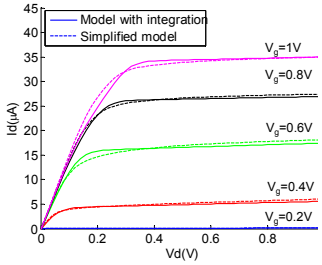

Fig. 2 Drain current output characteristics (Id vs Vd): (19,0), *tox*=1nm, *Lg*=10nm. λ_{ap} and λ_{op} are 500nm and 15nm, respectively. Solid line: SPICE model [3]. Dashed line: simplified model [6] for system optimization.

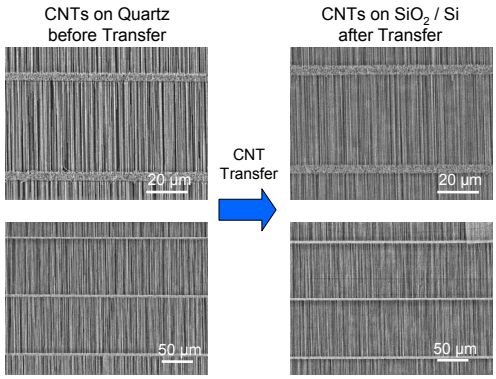

Fig. 4 Wafer-scale growth of aligned CNT on quartz (left). CNT alignment and density remains essentially the same after the transfer process [7].

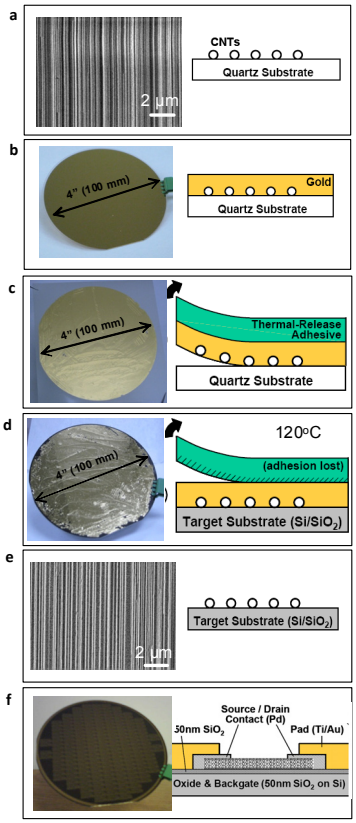

Fig. 5 Wafer-scale CNT transfer process [7].

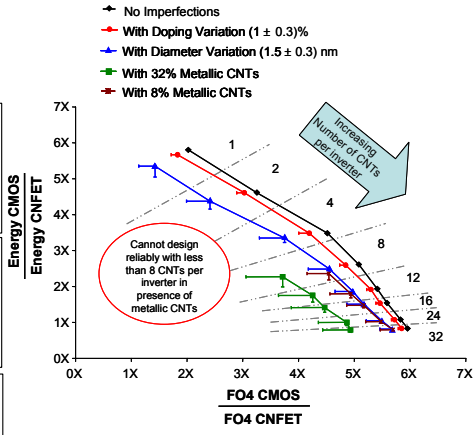

Fig. 3 Energy per cycle and FO4 delay improvement for CNFET inverter at 3σ points compared to 32 nm CMOS FO4 inverter. Error bars indicate 6σ points [4].

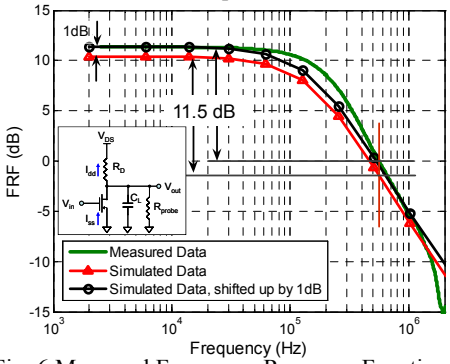

Fig. 6 Measured Frequency Response Function (FRF) of the CNFET common source amplifier (solid line, no symbol). Simulation using CNFET compact model [3] (solid line with "Δ"). Better match between model and measurement is achieved by shifting the model results up by 1 dB (solid line with "o") [9].

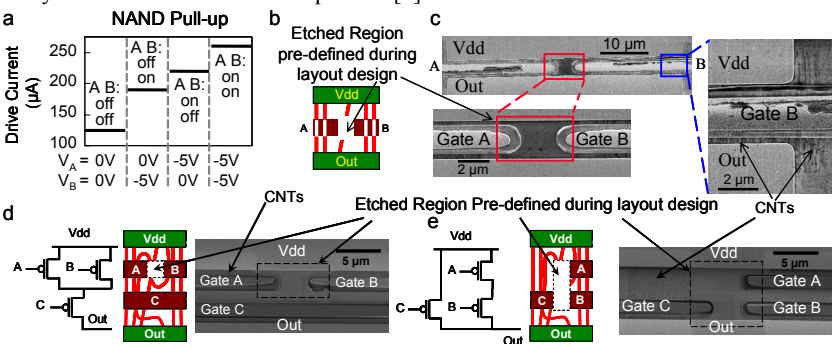

Fig. 7 Mis-positioned-CNT-immune logic structures on silicon after CNT transfer and without metallic-CNT burning. (a)-(c) NAND pull-up. (d) AND-OR-INVERT pull-up and (e) OR-AND-INVERT pull-up logic structures and SEM images. [7]

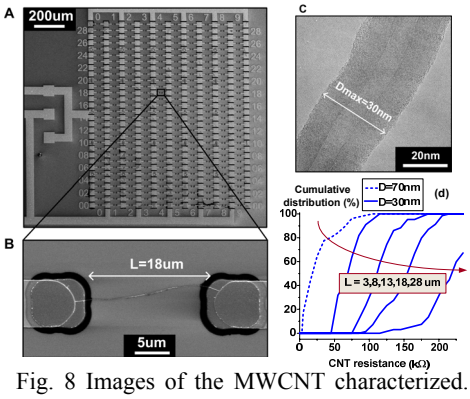

Fig. 8 Images of the MWCNT characterized. (A) SEM image of an array of MWCNT interconnects. (B) Close-up SEM image showing a 18μm-long individual MWCNT interconnect. (C) TEM image of a typical MWCNT with outer diameter ~ 30nm. (D) Statistical distribution of measured CNT resistance. [13]

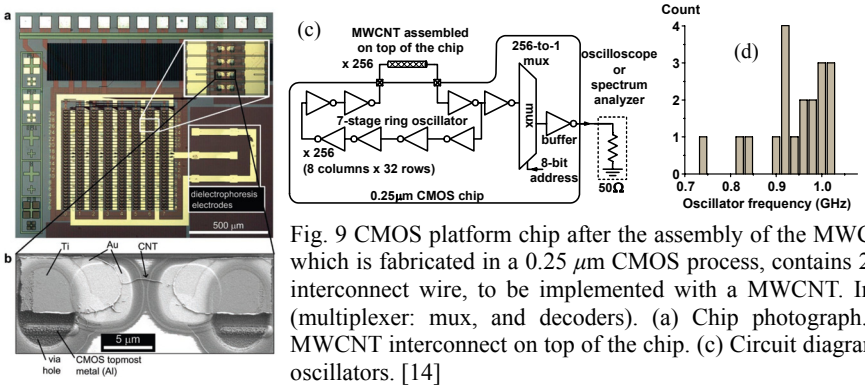

Fig. 9 CMOS platform chip after the assembly of the MWCNT interconnects on the chip surface. The chip, which is fabricated in a 0.25 μm CMOS process, contains 256 ring oscillators with an intentionally missing interconnect wire, to be implemented with a MWCNT. In addition, the chip contains selection circuitry (multiplexer: mux, and decoders). (a) Chip photograph. (b) Close-up SEM image of one fabricated MWCNT interconnect on top of the chip. (c) Circuit diagram (d) Measured oscillation frequency for 19 ring oscillators. [14]