Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 40-41

B-2-2

Compact Modeling of Ballistic Nanowire MOSFETs

Kenji Natori

University of Tsukuba , Institute of Applied Physics
Tsukuba, Ibaraki 305-8573, Japan
Phone: +81-298-53-5311, Fax: +81-298-53-5205 E-mail: natori@esys.tsukuba.ac.jp

1. Introduction

Recently the nanowire transistor attracts wide attention. In nanoscale devices where the quasi-ballistic or ballistic operation is dominant, further down-sizing may not be effective for performance improvement, or rather, it may bring about the off-current degradation due to the intensified short channel effect. The nanowire transistor in contrast, especially in the gate-all-around structure, allows close control of the channel current leading to the improved off-leak characteristics.

In this paper, we present a compact and reliable model of the ballistic nanowire MOSFET. It provides the device characteristics in the high performance limit where carrier scattering is eliminated. The model considers the subband effect as well as the quantum capacitance of the nanowire.

2. Compact Model

The current expression is already reported elsewhere [1][2], and only the essence is summarized. Similarly as in other ballistic transistors, the device current is controlled by the carrier flow at the bottleneck point close to the source electrode, as depicted in Fig. 1. When the energy of each subband extends sufficiently above the Fermi energies of the source and the drain (each denoted by μ_S and $\mu_D = \mu_S - V_D$), the device current is compactly expressed

$$I_D = G_0\left(\frac{k_BT}{q}\right)\sum_i g_i \ln\left\{\frac{1+\exp[(\mu_S - E_{i0})/k_BT]}{1+\exp[(\mu_D - E_{i0})/k_BT]}\right\}. \quad (1)$$

Here, $G_0 \equiv 2q^2/h = 77.8$ μS is the quantum conductance, g_i (i = 0, 1,…) is the degeneracy of the i-th subband, and E_{i0} stands for the minimum of the i-th subband at x_{max}. As for the device structure, two arrangements of the gate electrode are studied as in the cross section of the device in Fig. (2): One is the planar gate structure in figure (a), and the other is the Gate-all-around structure (GAA) in figure (b). The gate capacitance is respectively derived as

$$C_{GPL} = \frac{2\pi\varepsilon_{ox}}{\ln\left\{\frac{\sqrt{2r+t_{ox}}+\sqrt{t_{ox}}}{\sqrt{2r+t_{ox}}-\sqrt{t_{ox}}}\right\}}, \quad (2)$$

$$C_{GGAA} = 2\pi\varepsilon_{ox}\left[\ln\left(\frac{r+t_{ox}}{r}\right)\right]^{-1}. \quad (3)$$

In the planar gate configuration, the parasitic capacitance C_p associated with the backgate is also given by the similar expression. For evaluation of the device current I_D, we need the value $(\mu_S - E_{io})$, and the value is evaluated by electrostatics associated with the gate bias and the channel charge. Specifically, we can derive the relation

$$(V_G - V_t) - \alpha\frac{\mu_S - \mu_0}{q} = \frac{|Q|}{C_G} \quad (4)$$

where V_t is the threshold voltage, $\alpha \equiv 1 + C_p/C_G$, and μ_0 is the minimum energy of the lowest subband. The channel charge density Q is estimated from the carrier distribution in the subband as

$$|Q| = \frac{q}{\pi}\sum_i g_i\left[\int_{k_{i\min}}^{\infty}\left[1+\exp\left\{\frac{E_i(k)-\mu_S}{k_BT}\right\}\right]^{-1}dk + \int_{-\infty}^{k_{i\min}}\left[1+\exp\left\{\frac{E_i(k)-\mu_D}{k_BT}\right\}\right]^{-1}dk\right]. \quad (5)$$

Equations (1), (4), (5) as well as the gate capacitance in Eqs. (3) and (4) constitute a compact model for evaluation of the I-V characteristics of a nanowire MOSFETs, and one can evaluate I_D, if the subband parameters, the MOSFET structure and the applied biases are given.

4. Results

We try to evaluate the I-V characteristics of a silicon nanowire MOSFETs at room temperature with the use of the subband parameters of a silicon nanowire with $(1.34\ \text{nm})^2$ cross sectional area, reported by the Bologna University group[3](Fig. 3). Fig. 4 is the I-V_D characteristics for the case $r = t_{ox}$ =1 nm with the SiO_2 gate insulator (GAA). Cylindrical wire is assumed although the data in [3] is used. Current magnitude is around 30 μA. Fig. 5 is the I-V_G characteristics, and Fig. 6 is the same plot in a logarithmic scale. The gate-all-around structure gives the ideal S value of ~60 mV/dec. The drain conductance in Fig 7 is a broad increasing function. But the same conductance in low temperature (5K) shows characteristic structures. The step structure for V_D = 0 V show the quantum conductance steps of G_0 and $4G_0$ reflecting the subband structure. Notice that the magnitude of conductance is of the same order for room temperature and for low temperature. Characteristic effects

of the quantum capacitance and the temperature effect will also be discussed.

4. Conclusion

A simple but reliable compact-model of the nanowire MOSFET suitable for assessment of the device is disclosed. The application to a thin geometry silicon nanowire MOSFET reveals some characteristic features of the device.

Reference

[1] K. Natori, Y. Kimura, and T. Shimizu, J. Appl. Phys., vol.97. pp.0343061, (2005).

[2] D. Jimènez, J. J. Sáenz, B. Iniquez, J. Suné, L. F. Marsal, and J. Parllarès, J. Appl. Phys., vol.94. pp.1061, (2003).

[3] E. Gnani, S. Reggiani, A. Gnudi, P. Parruccini, R. Colle, M. Rudan, and G. Baccarani, IEEE Trans. Electron Devices, vol. ED-54, pp. 2243, (2007).

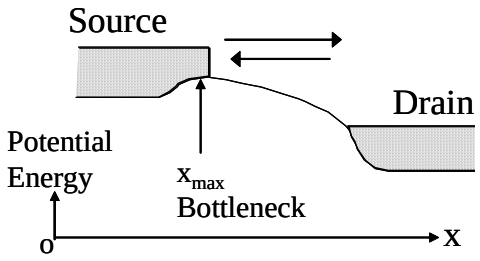

Fig. 1. Potential energy profile in the nanowire MOSFET along the channel.

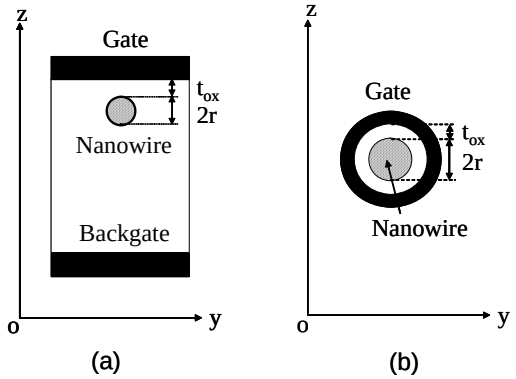

Fig. 2. Cross section of the nanowire MOSFET analyzed. (a) Planar gate structure. (b) Gate-all-around structure.

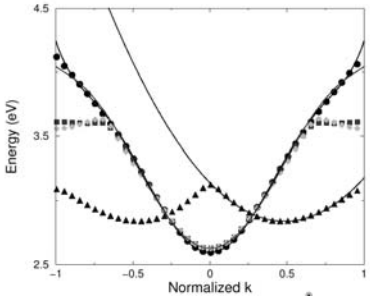

Fig. 3. The subband structure of the analyzed silicon nanowire MOSFET. [110]-square cross section with 1.34 nm side. Data is from DFT calculation and reported by E. Gnari et al.[3].

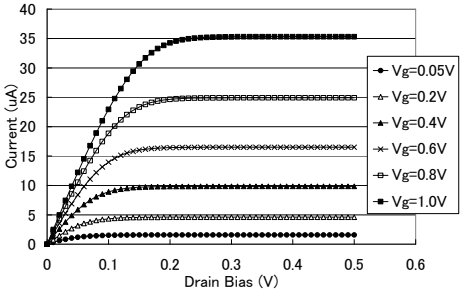

Fig. 4. I-V_D characteristics of the silicon nanowire MOSFET made of the nanowire in Fig. 3 at room temperature.

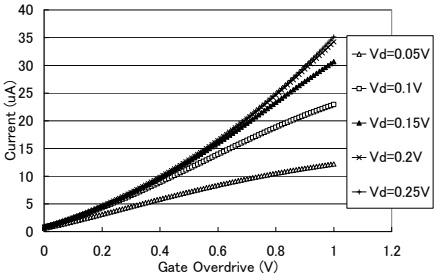

Fig. 5. I-V_G characteristics of the silicon nanowire MOSFET.

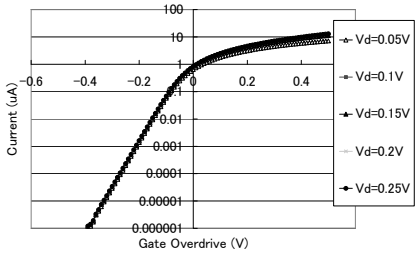

Fig. 6. I-V_G characteristics of the silicon nanowire MOSFET in logarithmic scale. The subthreshold S is 58 mV/dec.

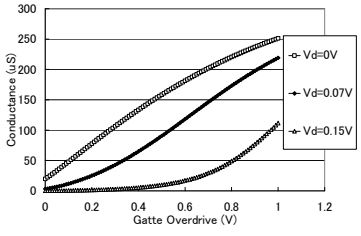

Fig. 7. Drain conductance at room temperature.

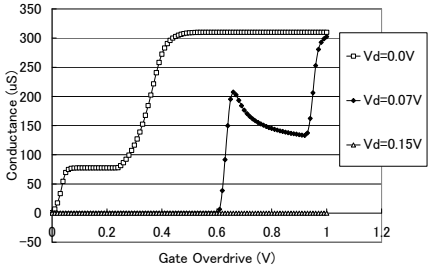

Fig.8. Drain conductance in low temperature (5K).