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Investigate the Effects of Channel Materials & Channel Orientations on the Performance of Nanowire FETs

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1. Introduction

One-dimensional Si nanowires (SiNWs) are extensively studied as they are promising building blocks in nanoelectronic and nanophotonic systems with good device performance [1]. Recent advanced development reveals that physical property of nanowires (NWs) could be modified depending on the NW growth direction and diameter. This suggests that material structure such as cross-sectional shapes and channel orientation play an important role in device performance optimization. Coupled with the fact that besides silicon, other semiconductor materials such as germanium (Ge) demonstrates promising results [2-4], a new chapter of study on alternate high mobility channels in nano world has opened. Hence, the objective of this work is to explore and compare ultimate performance of a set of cylindrical nanowire devices with different semiconductor materials (Si, Ge and GaAs) and channel orientation so as to make a judicious choice. We found that unlike UTB-FETs [6], for n-type (p-type) FETs, 3nm diameter GaAs (Ge) NW FETs always outperform the other cases regardless of the oxide thickness.

2. Approach

Firstly a $sp^3d^5s^*$ tight-binding (TB) approach [5,7] is employed to investigate the electronic properties of NWs in terms of E-k dispersion in order to accurately capture orientation effects as well as quantum effects in a nano scale system. Figure 2 shows the simulated 100 bands using $sp^3d^5s^*$ empirical TB model approach for three different channel materials: Silicon (Si), Germanium (Ge) and Gallium Arsenide (GaAs) with diameter of 3nm. The E-k diagrams shown in Figure 2 are for channel orientation [100]. Using similar approach, E-k relations for channel orientation of [110] and [111] for Si, Ge and GaAs are also generated for extensive performance evaluation.

Based on the calculated E-k dispersion, we engaged a semi-classical top-of-barrier MOSFET model [8] to evaluate the ballistic I-V characteristics of NW MOSFETs by self-consistently solving Poisson equation and the number of carriers at the top-of-barrier in order to evaluate the ultimate performance of these semiconductor NW FETs with various material properties.

3. Results and Discussion

Fig. 3 shows the Ids–Vds curves for n- and p-channel devices with Si, Ge and GaAs as channel materials with gate oxide thickness of 1.6nm and off-current at $20\mu A/\mu m\cdot(D)$ obtained from bandstructures from Fig. 2. For n-type NW FETs, Si, Ge and GaAs of [110] channel orientation gives the highest on-current. For p-type NW FETs, Si and GaAs of [110] channel orientation and Ge of [111] channel orientation give highest on-current. Moreover, for Ge and Si nanowire FETs, p-type device outperforms n-type which is contrary to the performance trends in conventional planar MOSFETs. This is due to lifting of degeneracy between light and heavy holes significantly by quantum confinement which reduces the average hole effective mass in the channel [2]. Fig. 4 and Fig. 5, respectively, compare output and transfer performance of NW devices of different channel materials in which the channel orientation with the highest on-current, as determined from Fig. 3, is chosen. We consider oxide thicknesses of 1.6nm and 0.5nm in Fig. 4a (5a) and Fig. 4b (5b), respectively. On-current increases as anticipated when the oxide thickness decreases due to better gate control. For example, on-current of GaAs was increased by 125% when the oxide thickness was reduced from 1.6nm to 0.5nm. In terms of channel material performance, GaAs outperformed Si and Ge for n-type NW FETs while Ge outperformed Si and GaAs for p-type NW FETs at the same oxide thickness. To further investigate the detailed device physics, carrier density and average velocity as a function of V_{GS} are shown in Fig. 6 and Fig. 7, respectively. In general, current is the product of average velocity and carrier density. For p-type devices, as the carrier density and average velocity follow the same trend, hence current also follows similar trend. For n-type devices, although the carrier density of GaAs is low, its injection velocity compensates for the low carrier density and results in the high ON-state current of GaAs NW FETs. The transconductance of p- and n- devices with these various material NW FETs are investigated in Fig. 8. For n-type devices, GaAs has the highest transconductance while for p-type devices, Ge has the highest transconductance. Fig. 9, furthermore, shows the I_{on}–t_{ox} plot for n-type and p-type NW FETs. Unlike UTB MOSFETs [6], GaAs for n-type and Ge for p-type have the highest on current regardless of oxide thickness, possibly due to the strong gate control in GAA systems. Finally, Table 1 shows the intrinsic device delay of these different material NW FETs with the channel length of 8nm. It also indicates GaAs[110] and Ge[111] NW FETs outperform the other n-type and p-type FETs, respectively.

4. Conclusions

In summary, we present the device performance of different channel materials and channel orientations in NW FETs. For n-type device, GaAs with [110] channel orientation and for p-type device, Ge with [111] channel orientation, respectively give the best performance. Moreover, similarly in UTB MOSFETs, p-type NW FETs outperform their n-type counterparts in case of Si and Ge. However, unlike in UTB MOSFETs, the best performing devices maintain their lead irrespective of the oxide thickness.

References

[1] N. Singh et al., IEEE Electron Dev. Lett., **27**(2006) 383. [2] J. Wang et al., *Internaltional Electron Device Meeting* (2005) 530. [3] Lieber C.M. et al., Nano Letters, **7(3)** (2007) 642. [4] Lieber C.M. et al., Nature **441(7092)** (2006) 489.[5] T.B. Boykin et al., Phys. Rev. B, **69** (2004) 115201. [6] A. Rahman et al., IEDM, (2005). [7] Website: http://nanohub.org. [8] A. Rahman et al., IEEE Trans. Electron Dev., **50** (2003) 1853.

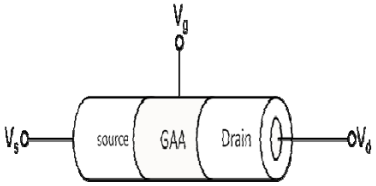

Fig. 1: A schematic of the simulated Cylindrical Nanowire FETs. The diameter of the Circular cross-section (D) is 3nm. The oxide thicknesses (tox) for this simulation are 0.5nm and 1.6nm.

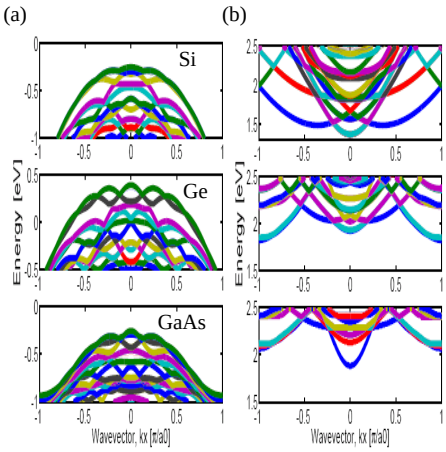

Fig. 2: (a) and (b) Simulated E-k diagram of valence and conduction band for channel orientation [100], respectively, for Si, Ge and GaAs using sp3d5s* empirical TB model.

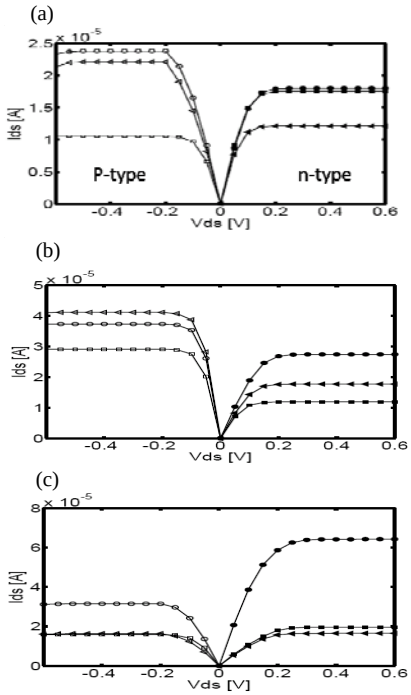

Fig. 3: Ids – Vds curves for (a) Si, (b) Ge and (c) GaAs NW FETs. The gate oxide thickness is 1.6nm and the off-current is set to 60nA at Vdd=0.6V. Square Symbols for [100] orientation, Circle Symbols for [110] orientation and Triangle Symbols for [111] orientation. For n-type device, the highest on-current is given by [110] channel orientation in all materials, while for p-type, the highest on-current is given by [110], [111] and [110] in Si, Ge, and GaAs cases, respectively.

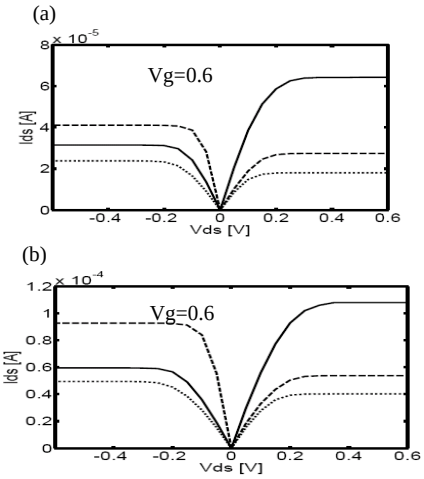

Fig. 4: Ids–Vds curves for Si (dotted line), Ge (dashed line) and GaAs (solid line) NW FETs at (a) tox=1.6nm and (b) tox=0.5nm. Ge NW FET outperforms the other two cases for p-type MOFETs while GaAs NW MOSFET outperforms the other cases for n-type MOSFETs.

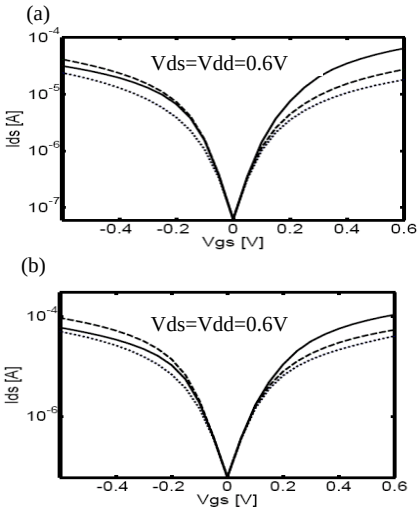

Fig. 5: Comparison of Ids – Vgs curves for Si (dotted line), Ge (dashed line) and GaAs (solid line)NW FETs at (a) tox=1.6nm and (b) tox=0.5nm.

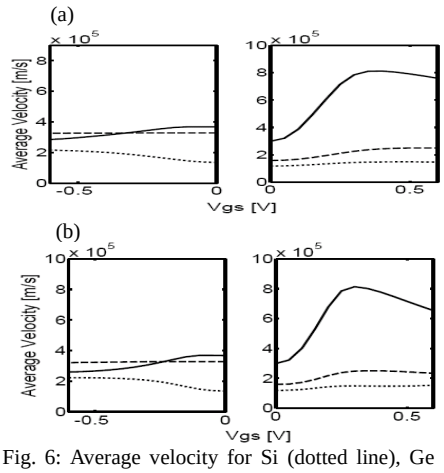

Fig. 6: Average velocity for Si (dotted line), Ge (dashed line) and GaAs (solid line)NW FETs for tox=1.6nm (a) and tox=0.5nm (b). GaAs has the highest electron average velocity while GaAs and Ge have similar hole average velocity.

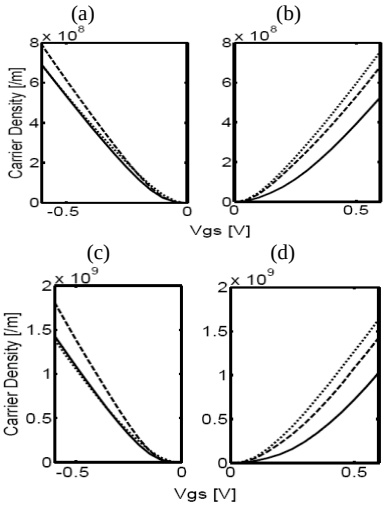

Fig. 7: Comparison of carrier density for Si (dotted line), Ge (dashed) and GaAs (solid line)NW FETs for tox=1.6nm for (a) n-type and (b) p-type and tox=0.5nm for (c) p-type and (d) n-type. Si has the largest electron density but Ge have the largest hole density.

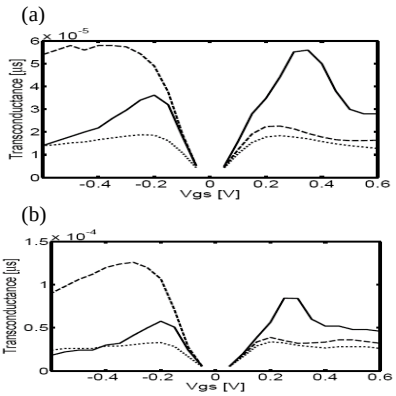

Fig. 8: Transconductance,gm curves for Si, Ge and GaAs NW FETs at (a) tox=1.6nm and (b) tox=0.5nm show Ge and GaAs give high gm, which agrees with high ON-current.

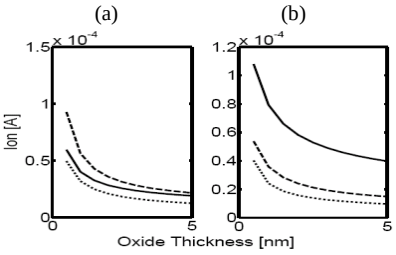

Fig. 9: Ion–oxide thickness curves for Si, Ge and GaAs for (a) p-type and (b) n-type. GaAs has overall high on-current for n-type while Ge for p-type.

Vdd=0.6V	Time delay (ps) @ tox=0.5nm & Lg=8nm					
	N-type			P-type		
	Si	Ge	GaAs	Si	Ge	GaAs
[100]	0.0486	0.0708	0.0503	0.0886	0.0344	0.0567
[110]	0.0521	0.0342	0.0122	0.036	0.0271	0.0308
[111]	0.0709	0.0536	0.0358	0.0374	0.025	0.058

Table 1: The intrinsic device delays for simulated n-type and p-type Si, Ge and GaAs nanowires for 3 channel orientations, [100], [110] and [111].