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Modeling and Analysis of Short-Channel Effects in Double-Gate MOSFETs

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1. Introduction

Double-Gate MOSFETs are considered to be a candidate for the next generation MOSFET structure [1]. A big advantage of such structure with a very thin silicon layer thickness is suppression of the short-channel effect even down to 10nm. To exploit the advantage for circuit applications, accurate compact models including the precise short-channel effect is inevitable.

Though the threshold voltage modeling including the volume inversion effect is well discussed [2], modeling of the subthreshold region, where the most feature of the DG-MOSFET is observable, is not done yet. Here we focus on the problem. With use of the model it is shown that the volume inversion effect improves the subtrehshold characteristics drastically, however, the enhanced improvement of the device characteristics are not obvious under the on-current condition.

2. Modeling the short-channel effect

Fig. 1a shows the studied DG-MOSFET and its device parameter values. Our focus is given on the subthreshold modeling as schematically shown in Fig. 1b. All symbols used in the following equations are summarized in Table 1. We start with the Poisson equation

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = -\frac{\rho(x,y)}{\varepsilon_{si}} \quad (1)$$

By approximating that the field to the device depth direction is homogeneous, we simplify the Poisson equation as

$$E_x(x,y) + W_d \frac{\partial E_y'(y)}{\partial y} = \frac{1}{\varepsilon_{si}} \int_0^{W_d} \rho(x,y)dx \quad (2)$$

By further approximating a triangle carrier distribution to the depth direction (see Fig. 2a) and linearly decreasing from source to drain (see Fig. 2b), the right hand side integration is written analytically. The final equation for the gate voltage shift ΔV_{gs} (see Fig. 1b) is derived with use of the Gauss low

$$\begin{aligned}
\Delta V_{gs} &= \frac{\varepsilon_{si}}{C_{ox}} \frac{T_{si}}{2} \frac{\partial E_y(y)}{\partial y} \\
&= \frac{\varepsilon_{si}}{C_{ox}} \frac{T_{si}}{2} (-A(sw3V_{gs} - V_{fb}) + \frac{qp_{p0}}{\varepsilon_{si}} + 2AV_{bi}) \\
&\quad \exp(-\sqrt{A}L_g\{1 - (sw1 + sw2(1 + \log(V_{ds})))\}) - sw4
\end{aligned} \quad (3)$$

$$A = \frac{\varepsilon_{ox}}{\varepsilon_{si}T_{ox}W_d} \quad (4)$$

Model parameters are introduced to compensate the approximations applied.

The developed model equations are implemented into HiSIM-DG, which solves the potential distribution along the silicon layer thickness explicitly as shown in Fig. 3 [3]. The accuracy of the calculated potential values are compared with 2D-device simulation results.

3. Results and Discussions

The calculated I_{ds}-V_{gs} subthreshold characteristics with the developed model are compared with 2D-device simulation results in Fig. 4 for various L_gs. It is seen that the developed model can reproduce 2D-device simulation results for different V_{ds} values. Fig. 5 compares calculated I_{ds}-V_{ds} characteristics and their derivatives with 2D-device simulation results. DG-MOSFET preserves relatively good features down to L_g=40nm as observed in g_{ds} characteristics. However, clear degradation of g_{ds} at higher V_{gs} is observed. This is obvious even for L_g=100nm.

It is known that DG-MOSFETs realize very good subthreshold characteristics. Fig. 6a compares the subthreshold swing with that of the bulk-MOSFETs as a function of L_g. It is seen that improvement is drastic. The subthreshold swing provides a measure of the short-channel effect. Thus it is verified that the short-channel effect is well suppressed in DG-MOSFETs.

Fig. 6b compares the length of the pinch-off region ΔL again as a function of L_g. This value verifies the strength of the gate control. Under the saturation condition, the high lateral electric field occurs at the drain side. V_{ds} increase causes further extension of the high field region into channel middle, resulting in the increase of ΔL. This value is dependent on L_g. Longer is L_g, longer is ΔL. By reducing L_g, thus ΔL reduces automatically as depicted by solid square symbols in Fig. 6b. However, the reduction of DG-MOSFETs in comparison to bulk-MOSFETs is not seen but stays nearly on the same line. This concludes that the structural advantage is not obvious in the gate control point of view. The gate control of the DG-MOSFET is improved by the two facing gates. However, the improvement is diminished with increased V_{ds}. The reason is attributed to the fact that the carriers exist away from the surface and gather in the middle of the substrate due to the volume inversion effect. Under the condition carriers are rather governed by the electric field induced by the drain voltage. This results in easy loss of the gate control.

4. Conclusions

We have developed a model describing the subthreshold characteristics. HiSIM-DG including the developed model was verified to reproduce 2D-device simulation results. It was found that the suppressed of the short-channel effect in the subthreshold region is diminished under the on-current condition.

References

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[2] H. Oka, R. Tanabe, N. Sadachika, A. Yumisaki, and M. Miura-Mattausch, *Jpn. J. Appl. Phys*. (2007) 2096-2100.

[3] N. Sadachika, H. Oka, R. Tanabe, T. Murakami, H. J. Mattausch and M. Miura-Mattausch, *Proc. SISPAD* (2007) 289-292.

Table 1. Explanation of symbols.

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x	direction along the channel
y	direction vertical to the channel
ϕ	potential
ρ	total charge density
ε_{si}	silicon permittivity
ε_{ox}	oxide permittivity
E	electric field
W_d	depletion width
T_{ox}	gate oxide thickness
T_{Si}	silicon layer thickness
N_{sub}	substrate impurity concentrarion
C_{ox}	oxide capacitance
V_{fb}	flat-band potential
V_{bi}	built-in potential
L_g	gate length
sw1-4	model parameters
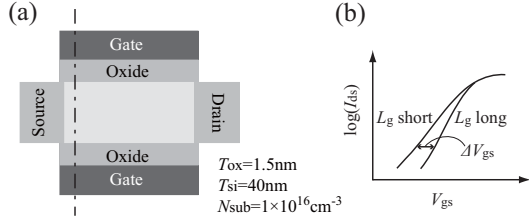
Fig. 1. (a) Studied DG-MOSFET and its device parameter values; (b) degradation of subthreshold swing with reduced gate length.
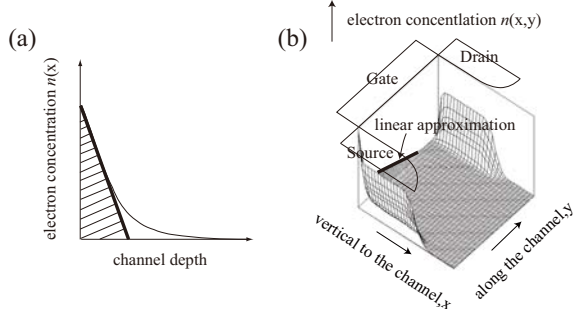

Fig. 2. Approximations applied for the carrier distribution; (a) to the depth direction, (b) to the channel direction.
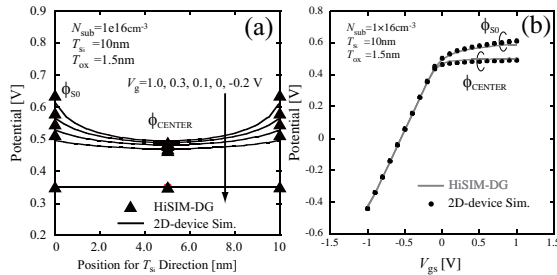

Fig. 3. Calculated potential values; (a) potential distribution along the line shown in Fig. 1a, (b) potential values at the surface and the middle of the silicon layer.
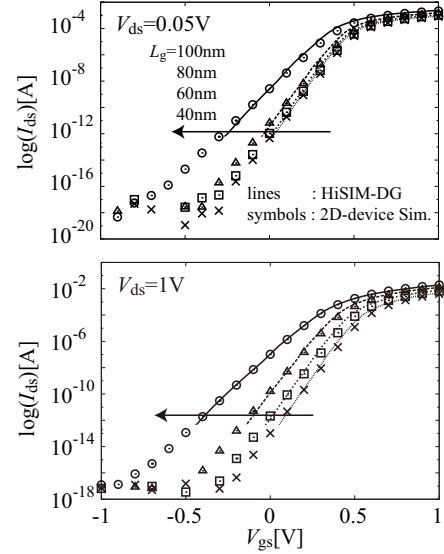

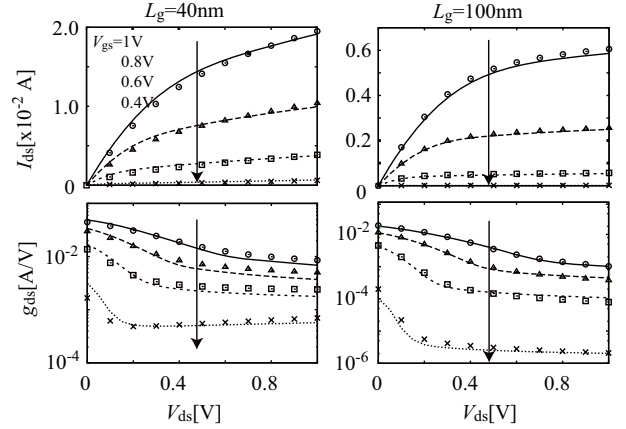Fig. 4. Comparison of calculated I_{ds}-V_{gs} subthreshold characteristics with 2D-device simulation results.

Fig. 5. Comparison of calculated I_{ds}-V_{ds} characteristics and their derivatives with 2D-device simulation results. Lines are HiSIM-DG results and symbols are 2D-device simulation results.
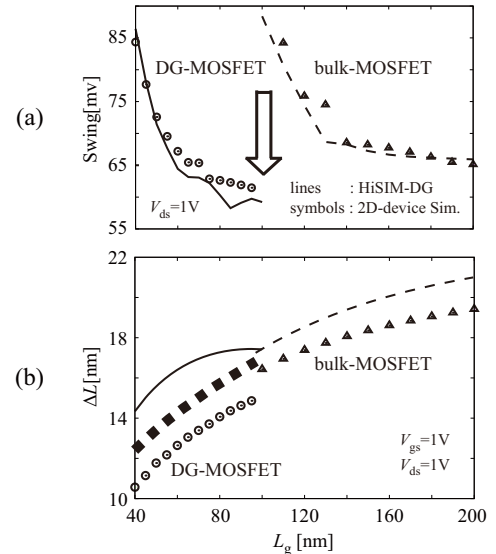

Fig. 6. (a) Subthreshold Swing as a function of L_g; (b) length of the pinch-off region ΔL as a function of L_g.