Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 254-255

B-3-1

Low GIDL Characteristics on Fin-FET with Source/Drain Extension Engineering for 22nm Node Low Power Devices

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Introduction

Fully depleted CMOS devices with thin silicon layer such as fin-FETs and Multiple Gate Field Effect Transistors (MuGFETs) are promising future devices owing to their low-power and high-speed operation. This is because the structure has several advantages, such as a reduced short channel effect, a low leakage junction current, and good subthreshold characteristics[1-4]. In this paper, we demonstrate low gate-induced drain leakage (GIDL) characteristics of fin-FET by optimizing for drain extension structure.

Experiments

Fin patterning is performed with using spacer defined patterning technique [5,6]. In-situ phosphorus doped poly-Si gate and SiN sidewall are applied for the fin-FET. Arsenic ions are implanted into the drain extension regions through oxide. It was optimized implantation condition to realize suitable drain overlap length (*Lov*) and depth profile (Fig.1). Ideal drain extension structure is analyzed by using process and device simulations.

Results and Discussion

For realizing ideal extension drain structure, 3-D process and device simulation is performed. Simulated structure is shown in Fig.2 (A). In figs.2 (B) and (C), two types of the arsenic profiles are compared. Drain structure (a) is implied as our proposal structure. The concept of the profile is to control low impurity concentration in the center of the fin body. In this structure (a), it is suppressed to become an amorphous in the center of the fin body by the implantation damage. A profile (b) is fabricated with high dose and high energy. The impurity concentration at the center of the fin film regions is increased with a high dose. It is anticipated that the high dose implantation ions bring about crystal damage and to be an amorphous.

Id-Vg characteristics of drain extension structure (a) and (b) are compared in Fig.3. GIDL is about 1 order difference. Figs.4(A) and (B) show current flows and lateral electric field of the drain regions both of the structures (a) and (b). Smaller current density and lower electric field (Vg=-0.2V) are recognize in the structure (a). These are the origin by the gradual junction profile at the drain edge region. Fig.5 shows roll-off characteristics of threshold-voltage (*Vth*) and S-factor. Roll-off is suppressed in the structure (a). Fig.6 shows GIDL and S-factor of the fin-FET as a function of *Lov*. At the same *Lov*, low GIDL is realized in the structure (a) as the comparison that in the structure (b). *Lov* is changed by the thickness of the through oxide for the extension implantation steps. From the results, the structure (a) has high potential for the tolerance of process fluctuation. The maximum lateral electric field (*Ex*) of the structure (a) is lower than that of the (b) (Fig.7).

Figs.8 and 9 show a SEM photograph of the bird's-eyes view of the fin-FET after gate patterning and a TEM photograph of the fin-FET. Fin width and height are ~15nm and 50nm. Steep shapes of the fin and gate are realized by optimized each processes. Fig.10 shows measured extension resistance distributions as the function of arsenic dose. In low dose case, resistance distribution is not so large. On the other hand, in high dose case, the number of abnormal chips of high resistance is increased. This is prospected that an amorphous region by ion implantation could not recovered and changed to the polysilicon. Fig. 11 shows the measured *Id-Vg* characteristics of the fin-FETs with the structure (a). Gate length (*Lg*) of the fin-FET is 25nm. Low GIDL (~$1x10^{-11}$uA/um) and low DIBL (N/P=100/90mV) are realized. From these results, the structure of the fin-FET has a high potential for the application of low standby power devices.

Conclusion

Fin-FET with gradual source/drain extension profile was analyzed with device simulation. It is demonstrated that low GIDL, steep S-factor and suppression of roll-off characteristics are shown with practical fabrication process. This technology is one of the candidates of 22nm node LSTP devices for emerging generations.

References

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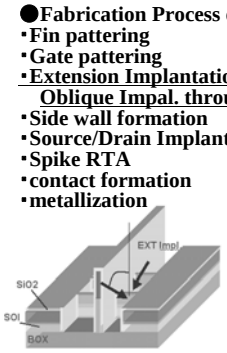

Fig.1 Fabrication process flow of fin-FET.

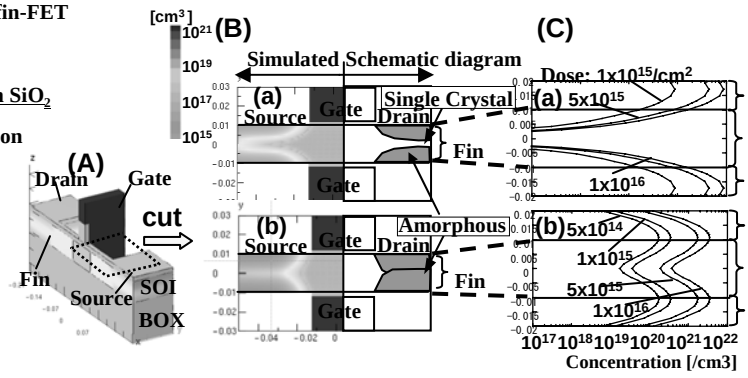

Fig.2 (A) Simulated structure of the fin-FET. (B) Simulated arsenic distributions of the drain extension edge regions. Top views. (C) Simulated arsenic depth profiles at source/drain regions.

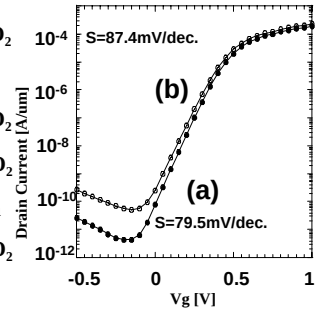

Fig.3 Simulated Id-Vg characteristics of fin-FET with the two types of extension profiles. Lg=25nm.

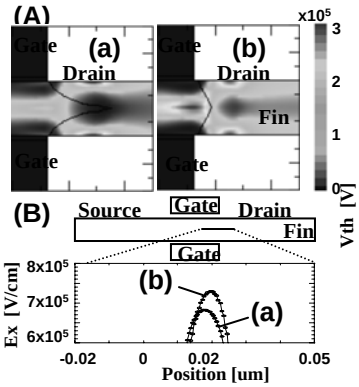

Fig.4 (A) Current density distributions of the two types fin-FETs. Vg=-0.2V, Vd=1.2V. (B) Lateral Electric field (Ex) at the drain edge.

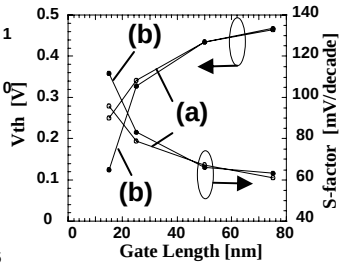

Fig.5 Vth and S-factor roll off characteristics of the two types of fin-FETs.

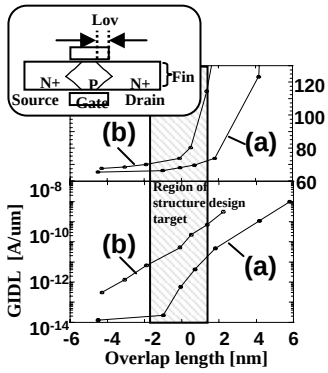

Fig.6 GIDL and S-factor of the two types of fin-FETs as a function of overlap length (Lov).

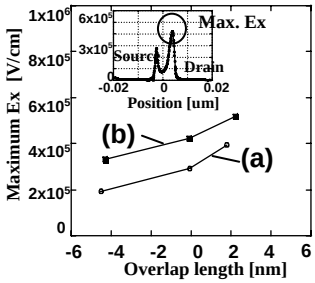

Fig.7 Comparison maximum lateral electric field (Ex) between (a) and (b) as a function of Lov. Vg=Vd=1.2V.

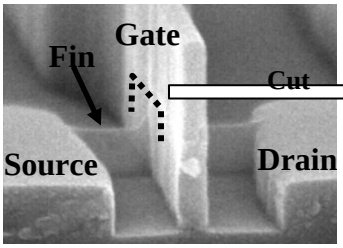

Fig.8 SEM photograph of the bird's-eyes view of the fin-FET after gate patterning.

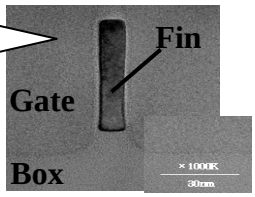

Fig.9 TEM photograph of the fin-FET. Thickness and height of the fin are 15nm and 50nm, respectively.

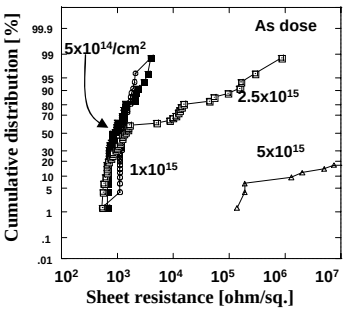

Fig.10 Measured Sheet resistance distributions depend on the arsenic implantation dose.

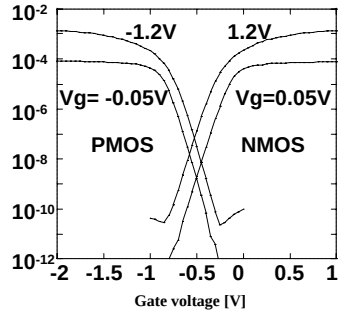

Fig.11 Measured Id-Vg characteristics of the fin-FETs. Low GIDL is realized by optimized drain structure. Lg=25nm