Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 256-257

B-3-2

Physical and Electrical Design of FinFET based SRAM Bitcell for 22nm Node and Below

S. C. Song, M. Abu-Rahma, B. M. Han, S. S. Yoon, J. Wang, W. Yang[1], C. Hu[1], and G. Yeap
Qualcomm Incorporated, San Diego, CA 92121, United States
[1] Electrical Engineering Dept., University of California, Berkeley, CA 94720 United States
Phone: 512-623-3889, e-mail: ssong@qualcomm.com

Abstract

Physical layout and electrical parameters of FinFET based SRAM bitcell have been systematically evaluated. Optimization flow of FinFET SRAM bitcell is also presented. Scaling contact related design rule is found to be the most important to achieve high layout density from FinFET bitcell. Significantly larger effective width relative to conventional planar device enables ultra high speed bitcell with still maintaining high density bitcell size. Due to superior electrostatic control, stand-by leakage current of FinFET bitcell is also kept low.

Introduction

FinFET technology and its variants have been widely accepted as an alternative device structure for ultra deep sub-micron device region, especially below 32nm nodes, owing to stronger electrostatic control of the channel (thus better short channel control) and potentially higher layout density [1, 2]. SRAM bitcell is considered as a first functional block in SOC to be implemented using FinFET, as critical issues of SRAM bitcell scaling, such as demand for continuous bitcell size scaling and electrical stability problem, can be resolved [3]. Highly repetitive nature of bitcell array layout also allows easier FinFET manufacturing at earlier stage [4]. Several previous studies published on FinFET based SRAM bitcell [5, 6], however, lack systematic evaluation of physical layout and electrical parameter optimization. We propose in this paper a systematic method to optimize FinFET bitcell in terms of bitcell size and electrical performance. Si based BSIM-MG model library [7] was used for this study

Results and Discussion

Example of SRAM bitcell layout for planar transistor is shown in Fig. 1 (a). FinFET SRAM bitcell layout is created by replacing planar transistors with FinFET in the planar bitcell (Fig. 1(b)). Contact landing pads are used on source/drain (S/D) of FinFET, which is slightly larger than contact itself for process margin. When FinFET is used, bitcell size is no longer dictated by width of Pull-Down (PD) transistor, but rather limited by contact size. FinFET bitcell, therefore, scales more aggressively with contact size reduction (Fig. 2 (a)). Due to inherent quantization of effective width (W_{eff}) of FinFET array and minimum area required for individual Fin pitch, number of Fins and corresponding W_{eff} make stair shape transition with continuous scaling contact size (Fig. 2 (b)). Ratio between Fin height and pitch determines efficiency of layout area utilization of FinFET. When Fin height/pitch (H/P) = 1/1, W_{eff} of FinFET becomes 2X of planar device width (i.e., W_{eff}/W_{planar} = 2). Higher H/P ratio increases layout efficiency (Fig. 3) [8] in general cases. When Fin geometry is limited by contact size, however, it's important to optimize Fin height and pitch along with minimum contact size allowed in the bitcell for the highest area efficiency. Fig. 4 shows (a) W_{eff} and (b) area efficiency comparison of two sets of Fin configuration in the same range of contact size. When minimum contact size is 30nm (with 10nm margin to S/D contact pad on each side), Fin configuration with H/P = 60/30 is better than Fin with H/P=70/40, not only because of higher H/P ratio, but also 2 Fins allowed at 30nm pitch. When min. contact size is 40nm, however, Fin with H/P=70/40 is more appropriate as it has higher W_{eff} and thus higher area efficiency. In order to systematically optimize Fin configuration limited by contact size, analytical equation for maximum W_{eff} calculation was derived (Fig. 5) using layout and process specific input parameters, such as contact size (including margin to landing pad), Fin thickness, Fin to Fin space and S/D implantation angle.

When bitcell layout is optimized, then electrical optimization of FinFET bitcell should be followed. Fig. 6 shows working flow for holistic FinFET SRAM bitcell optimization. Bitcell layout is optimized first, minimizing area based on design rules and process margin. Input parameters for equation in Fig, 5 are then used to optimize FinFET in the bitcell that requires strongest driving capability (with min L_g). Example of layout information and electrical parameter targets for FinFET bitcell is shown in Fig. 7. Within allowed maximum width for Fin array, configuration for PD transistor is determined that needs highest drive current. Optimization of Pass-Gate (PG) transistor using Static noise margin (SNM) and Write margin (WM) target is shown in Fig. 8. SNM and WM were simulated using different PG FinFET configurations with same set of Fin thickness (T_{fin}) and gate length (L_g) matrix of Pull-Up (PU) transistor. Each "fishing-net" in Fig. 8 indicates particular PG configuration with matrix of PU configurations. When multiple fishing-nets (thus multiple PG configurations) meet SNM and WM target, PG with higher I_{cell} (or I_{read}) is preferred (PG3 in the figure). Following PU optimization is shown in Fig. 9. Only part of selected fishing-net is in the spec window, indicating particular sets of PU T_{fin} and L_g meet the SNM and WM targets (as highlighted in the inset). PU FinFET configuration with minimum cell stand-by current (I_{stby}) is selected among various L_g and T_{fin} configurations of PU within the window. Fig. 10 shows final optimized FinFET configurations in SRAM bitcell using work flow described in Fig. 6 and layout/device spec in Fig. 7. Statistical optimization of bitcell stability to lower minimum operating voltage (Vccmin) is also important, and currently under further study.

Conclusion

We presented systematic method of FinFET SRAM bitcell optimization. Design rules related to contact are most important to scale FinFET bitcell. Optimum contact size for the maximum layout efficiency depends on Fin geometry (Fin height and pitch). Significantly larger effective width of FinFET enables ultra high speed bitcell with high density bitcell size. Stand-by leakage current of FinFET bitcell is also kept low.

Reference

[1] J. Kavalieros, et al., VLSI 2006 (7.1) [2] H. Shang, et al., VLSI 2006 (7.3) [3] A. Bansal, et al., IEEE TED p. 1409, 2007 [4] C. Hu, Future-Fab, Issue 23, 2007 [5] S. Inaba, et al., IEDM 2007 (18.6) [6] L. Witters, et al., VLSI 2005 (7A.1) [7] M.V.Dunga, et al., VLSI 2007 (4B.4) [8] S. Tang, et al., ISSCC 2001 (7.4)

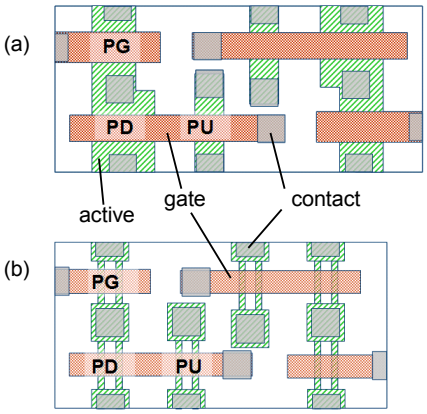


Fig. 1 Example of SRAM bitcell layout for (a) planar and (b) FinFET. PG, PD and PU stand for Pass-Gate, Pull-Down, and Pull-Up transistor. Planar transistors in the bitcell are replaced by FinFET. Contact landing pads are used on S/D of FinFET.

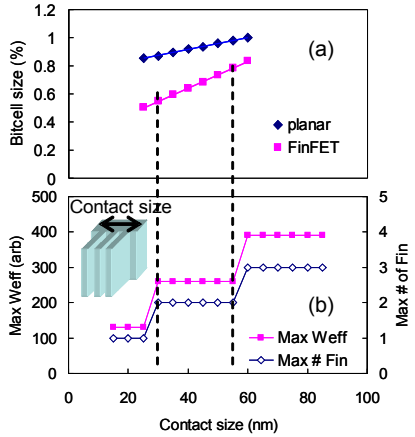


Fig. 2 (a) Bitcell size scaling with respect to contact size scaling for planar and FinFET. (b) Maximum number for Fin allowed and corresponding effective width (W_{eff}) of FinFET array according to contact size.

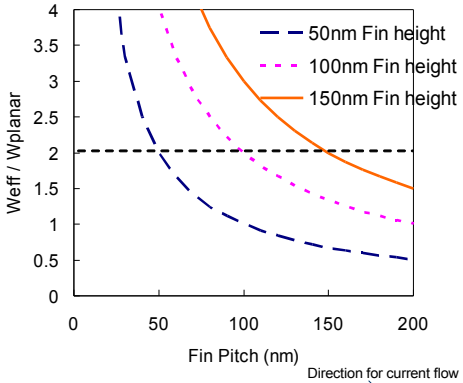
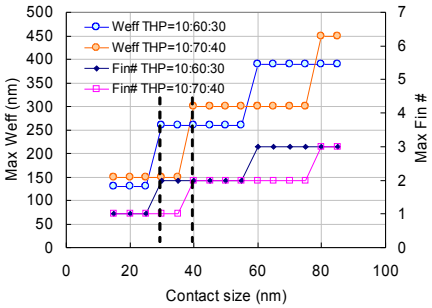


Fig. 3 Efficiency of layout area utilization of FinFET with respect to pitch of Fin array. When Fin height : pitch = 1 : 1, effective width of FinFET becomes 2X of width of planar device.



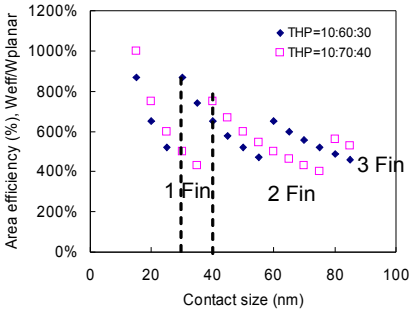
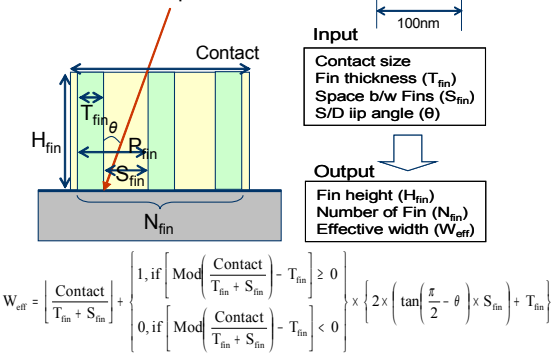


Fig. 4 (a) Maximum effective width (W_{eff}), maximum number of Fin, and (b) layout area efficiency for two different Fin configurations with respect to contact size. T:H:P stands for Fin thickness, height and pitch. Due to granularity of Fin pitch, maximum number of Fin forms rising stair shape (thus corresponding W_{eff}). Depending on the range of contact size, optimum Fin height and pitch can be determined. At constant Weff region, minimizing contact size maximizes area efficiency.



$$W_{eff} = \left\lfloor \frac{Contact}{T_{fin} + S_{fin}} \right\rfloor + \begin{cases} 1, if \left[Mod\left(\frac{Contact}{T_{fin} + S_{fin}} \right) - T_{fin} \right] \geq 0 \\ 0, if \left[Mod\left(\frac{Contact}{T_{fin} + S_{fin}} \right) - T_{fin} \right] < 0 \end{cases} \times \left\{ 2 \times \left(\tan\left(\frac{\pi}{2} - \theta \right) \times S_{fin} \right) + T_{fin} \right\}$$

Fig. 5 Analytical equation of effective width using process specific input parameters. “Floor” function is used to describe stair shape of W_{eff} with respect to contact size.

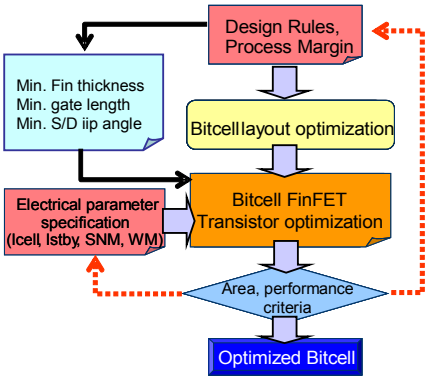


Fig. 6 Flow for FinFET SRAM bitcell optimization. Bitcell layout is optimized first minimizing area based on design rules and process margin. Input parameters for eq. in Fig, 5 are then used to optimize individual FInFET in the bitcell.

Layout information	
Contact size	40nm
Margin to S/D landing pad	5nm each
max width for Fin array	50nm
S/D implantation angle	30◦
Device Spec	
SNM	>220mV
WM	>235mV
Icell	>65uA/cell
Istby	<25pA/cell

Optimized bitcell				
	Lg (nm)	Tfin (nm)	Hfin (nm)	Nfin
PD	30	10	35	2
PG				
PU				

Fig. 7 Layout information and electrical parameter targets for FinFET bitcell transistor. Based on the layout information, FinFET configuration for PD transistor is determined.

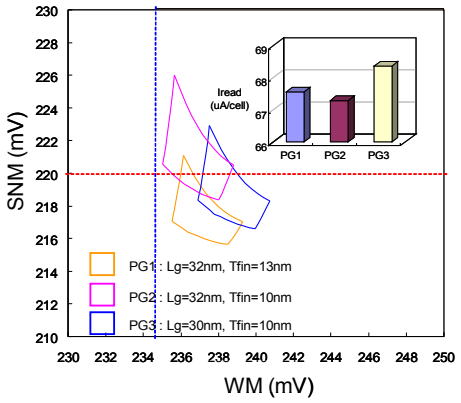
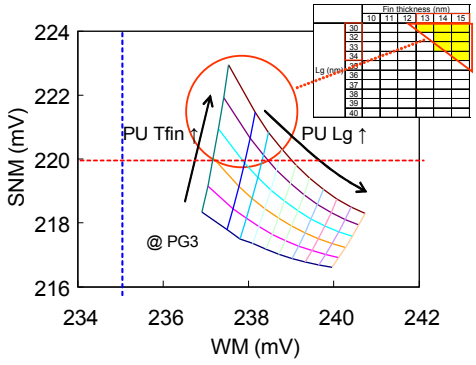


Fig. 8 Optimization of PG transistor using SNM and WM target. SNM and WM were simulated using different PG FinFET configurations with same set Tfin and Lg matrix of PU FinFET. When multiple PG configurations meet SNM and WM target, PG with higher I_{cell} (or I_{read}) is preferred.

Fig. 9 Optimization of PU transistor using SNM and WM target. When optimum PG transistor is determined, pairs of L_g and T_{fin} of PU FinFET meeting SNM and WM target are selected. Among various L_g and T_{fin} configurations of PU transistor within SNM and WM target window, PU FinFET configuration with minimum I_{stby} and/or maximum process margin is preferred.



Optimized bitcell				
	Lg (nm)	Tfin (nm)	Hfin (nm)	Nfin
PD	30	10	35	2
PG	30	10	35	2
PU	35	15	35	2

Fig. 10 Optimized FinFET configurations in SRAM bitcell using work flow described in Fig. 6 and layout/device spec in Fig. 7.