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Gate-All-Around 4-nm Silicon Nanowire Schottky Barrier MOSFET with 1-D NiSi Source/Drain

J. W. Peng[1, 2, 3], S. J. Lee[2, *], G. C. Albert Liang[2], N. Singh[1], C. M. Ng[3], G. Q. Lo[1] and D. L. Kwong[1]

[1]Institute of Microelectronics, 11 Science Park Road, Science Park II, Singapore, 117685
[2]Silicon Nano Device Lab, ECE Dept., National University of Singapore, 117576 Singapore
[3]Chartered Semiconductor Manufacturing Ltd., Singapore, 738406
Phone: +65 6516-6140, Fax: +65 6779-1103, *E-mail: elelsj@nus.edu.sg

1. Introduction

Schottky-Barrier (SB) MOSFET (SBFET) has attracted a renewed interest due to its inherent advantage of scalable to sub-10-nm-gate-length regime [1]. However, it is suggested that the S/D Schottky Barrier Height (SBH) should be less than 0.1 eV in order to have comparable current drivability as the conventional p/n-doped S/D MOSFET [2], and the reported SBH of the PMOS candidate, PtSi is ~0.2 eV, NMOS candidate, ErSi and YbSi are ~0.27-0.36 eV [1]. In view of lack of silicide with sufficiently low SBH at present, it is important to turn the efforts to minimize the SB width to increase the overall current.

Here, we demonstrate high performance SB-PFET as a result of the improved tunneling current in a novel Gate-All-Around (GAA) Si-Nanowire (SiNW) with 1-D NiSi Schottky contact architecture. The GAA SiNW with mid-band gap NiSi S/D SB-PFET demonstrates excellent device characteristics in terms of small Sub-threshold Slope (SS) (79 mV/dec on a 4-nm SiNW and 86 mV/dec on a 12.5-nm SiNW) and large I_{on}/I_{off} ratio (> 10^5).

2. Experimental

The process flow of GAA SiNW NiSi SB-MOSFET is shown in Fig. 1. SiNW is formed by self-limited oxidation of the Si-fin in dry O_2 as previously reported [3], and then 100-nm LPCVD α-Si was deposited on thermally grown 5-nm oxide, followed by implantation with P/4×10^{15} cm^2/25 keV and activation (1050 ^oC, 10s). The poly-Si gate was patterned to have the edges of SiNW exposed for silicidation. An optimized etching processing with selectivity of poly-Si over oxide > 20 was used to ensure no attack on SiNW during poly over etching. Subsequently, 100 Å SiO_2 / 150 Å SiN stack was deposited and etched to form a thin spacer. Then 1-nm Ti / 9-nm Ni was sputtered and formed silicide at the exposed SiNW and S/D pads by rapid thermal annealing (RTA) at 500 ^oC, 30s. Excess metal was removed subsequentially. Standard metal contact formation was done before the measurement. Fig. 2 (a) shows the sketch of final device structure, with the NiSi intentionally encroached towards the edges of the channel as a result of the diffusion of NiSi along SiNW [4]. Fig. 2 (b) and (c) show the TEM image of a 4-nm diameter and a 12.5-nm width SiNW cross section.

3. Results and Discussion

Fig. 3 shows the current-voltage characteristics of a 12.5-nm, 850-nm Lg device at zero gate bias, from which the hole mobility is calculated to ~233 cm^2/V.s [5], well agreed with Samsung's work and indicates good quality of SiNW [6]. Fig. 4 shows the I_d-V_g characteristics of three NiSi SBFETs on a single wafer and the device parameters of these three devices are listed in Table 1, along with the theoretical SS of a 4-nm Si body SOI top-gated SBFET [7]. As shown in Table 1, GAA SiNW SBFETs demonstrate smaller SS and larger on-state current (after normalization). Since SS is a robust measurement of the carrier injection in SBFET [7], the smaller SS suggests the carrier injection has been greatly improved. This improvement is significant in view of the SS of a 12.5-nm width SiNW SBFET out-performed of the theoretical SS of a 4-nm Si body SOI with the same T_{ox} (~150 mV/dec) [7]. Fig.5 shows the un-normalized transconductance of the 4-nm and 12.5-nm GAA SiNW devices. The maximum G_m of the 4-nm-diameter SiNW SBFET is surprisingly higher than the 12.5-nm width SiNW, suggests the current is less suppressed in the 4-nm diameter SiNW. Fig. 6 shows the effective-SBH extracted from the thermionic model. The effective-SBH of the 12.5-nm diameter SiNW drops much faster than that of the corresponding top-gated SOI planar SBFET, which indicates the tunneling current dominate the overall current faster in GAA SiNW SBFET.

The potential profile at the source SB at on-state is shown in Fig. 7 and the barrier thickness as a function of SOI body thickness and SiNW diameter is shown in Fig. 8. These two graphs clearly show the advantage of GAA SiNW architecture in SBFET design on SB thickness reduction and the use of this architecture is a mean to strongly improve the electrical characteristics of SBFETs.

3. Conclusions

In conclusion, we have demonstrated good electrical characteristics on GAA SiNW NiSi SBFETs and the good device performance is attributed to the improved carrier injection as a result of using GAA SiNW architecture.

References

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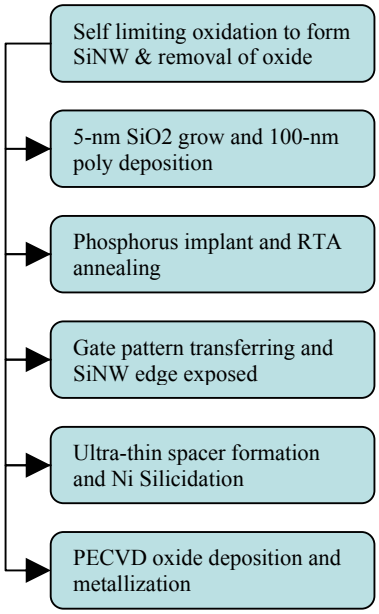

Fig. 1: Process flow of the GAA SiNW NiSi Schottky barrier MOSFETs

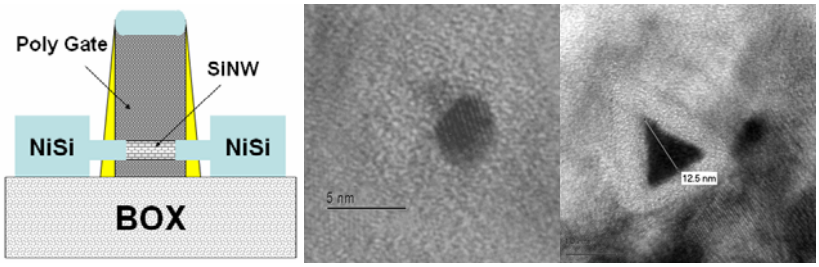

Fig. 2: (a) estimated final device structure of GAA SiNW NiSi SB-MOSFET, with NiSi encroached through the thin spacer (< 25-nm). (b) TEM image of a 4-nm diameter SiNW cross section. (c) TEM image of a 12.5-nm width SiNW cross section. Gate oxide thickness is ~5nm.

	4-nm SiNW	12.5-nm SiNW	1-um width, 100-nm Si TG SOI	4-nm TG SOI (reference 7)
T_{ox} (nm)	5	5	5	5
L_g (nm)	150	850	850	--
SS (mV/dec)	79	86	442	~150
I_{on} (μA)	0.83	0.36	0.33	--
I_{off} (pA)	0.36	0.17	1100	--

Table 1: Device parameters of the GAA SiNW and top-gated SOI planar NiSi SB-PFETs in Fig. 4

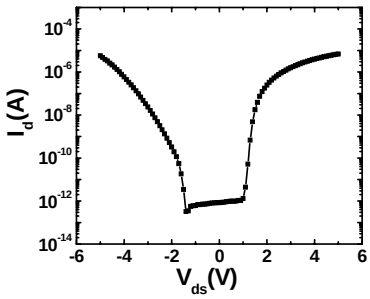

Fig. 3: Current-Voltage characteristics of a 12.5-nm GAA SiNW at zero gate bias. The total resistance obtained at large gate bias is 0.3486 MΩ and the fitted carrier density is 7.26E18 cm^{-3} according to the method in reference 5.

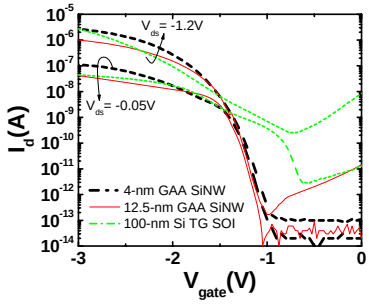

Fig. 4: Id-Vg characteristics of three devices on a single wafer: a 4-nm and a 12.5-nm diameter GAA SiNW and a 1-um width, 100-nm Si body SOI top-gated planar device. Device parameters are shown in Table 1.

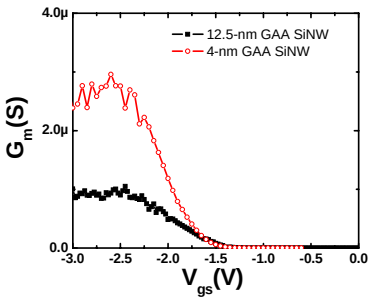

Fig.5: The transconductance of the 4-nm-diameter and 12.5-nm-diameter GAA SiNW in Fig. 4. Both increases as gate bias increases negatively and become a constant when gate bias is negatively larger than certain value.

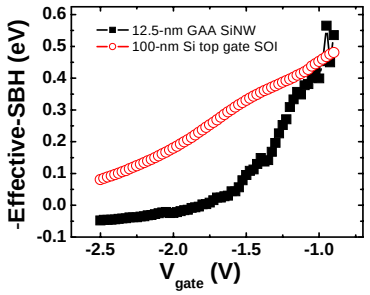

Fig.6: Effective-SBH of the 12.5-nm diameter GAA SiNW and the 1-um width, 100-nm Si top-gated SOI planar SBFET as a function of gate bias.

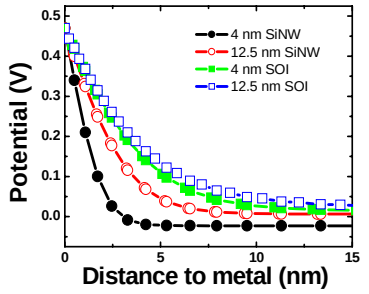

Fig.7: Calculated potential profile of the SB at on-state. The circle ones represent the GAA SiNW and the square ones represent top-gated SOI SBFET.

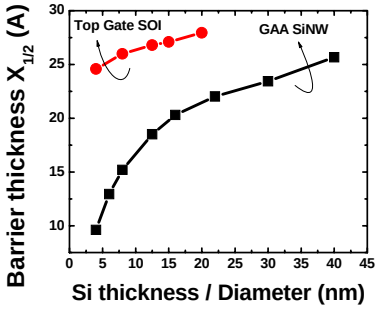

Fig.8: Calculated Full-Barrier-Width at Half Maximum ($X_{1/2}$) as a function of the Si body thickness of top-gated SOI planar devices and GAA SiNW diameters.