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Erbium/Platinum silicided Gate-All-Around Silicon Nanowire Schottky Source/Drain MOSFETs

EJ Tan[1,2,3], KL Pey[1,*], N Singh[2], GQ Lo[2], DZ Chi[3], YK Chin[1], LJ Tang[2]
[1]School of Electrical and Electronic Engineering, Nanyang Technological University, Nanyang Avenue, Singapore 639798, *E-mail: eklpey@ntu.edu.sg. [2]Institute of Microelectronics, 11 Science Park Road, Singapore Science Park 2, Singapore 117685. [3]Institute of Materials Research and Engineering, 3 Research Link, Singapore 117602.

INTRODUCTION Schottky source/drain (S/D) MOSFET (SBMOS) architecture in which the metallic source and drain region are in direct contact with the transistor channel can reduce S/D parasitic resistance as well as provide abrupt junction interfaces [1]. 'Top down' Nanowire transistors [2,3], due to enhanced drive current and better controllability of the channel potential, when fabricated with Schottky barrier source/drain, have been proposed as an ideal future transistor architecture [4]. In this paper, we demonstrate high performance CMOS silicon nanowire transistors with metal silicided nano-junctions (SBNWMOS) and gate-all-around (GAA) channel using Er-/Pt-silicide as the S/D material. The results demonstrate that effective scaling down of transistor dimensions down to 5nm is possible with SBNWMOSs.

DEVICE FABRICATION Fig. 1 shows the process flow and schematics of GAA SBNWMOS fabrication. The process is similar to the previously reported back-gated $ErSi_{2-x}$ SBNWMOS [5] up to self-limiting oxidation. Next, the gate was defined by patterning 9nm SiO_2/130nm α–Si stack, which was followed by 35nm wide Si_3N_4 spacer formation as shown in Fig. 2(a). Er (for N-SBNWMOS) and Pt (for P-SBNWMOS) silicidation was next carried out to form the metal silicide (MSi) S/D as shown in the schematic in Fig. 1. Fig. 2(b) shows the completed $ErSi_{2-x}$ SBNWMOS after silicidation and unreacted metal etch. Fig. 3(a) shows a cross-sectional TEM (XTEM) micrograph across the gate electrode. The micrograph confirmed that the wire sizes are ~5nm (bottom) and ~8nm (top). Fig. 3(b) shows a higher magnification XTEM micrograph of the bottom SiNW, which shows the nanowire surrounded by 9nm thermally grown SiO_2.

RESULTS AND DISCUSSION Fig. 4 shows the I_d-V_g and I_d-V_d curves of the GAA $ErSi_{2-x}$ and PtSi SBNWMOS with gate lengths (L_g) of 90nm. The $ErSi_{2-x}$ N-SBNWMOS I_{on} = 464μA/μm at V_d = 1.2V. The SS is 79mV/decade, with a DIBL of 53mV/V. The I_{on}/I_{off} ratio is ~1.1 X 10^5 measured at V_d= 50mV, with V_t = 0.14V. The PtSi P-SBNWMOS I_{on} = 618μA/μm at V_d = 1.2V. The SS is ~60mV/decade, with a DIBL of 10mV/V. The I_{on}/I_{off} ratio is ~5.6 X 10^5 measured at V_d = -50mV, with V_t = -0.3V. The SS, DIBL and overall characteristics for both the N and P-SBNWMOS are comparable/better than most reported SBMOS values [1, 6, 8-11]. The reasons for the excellent characteristics are believed to be due to the improved electrostatics of the GAA channel [2] as well as Schottky Barrier thinning [7] at the metal-semiconductor junction. The I_d-V_d characteristics in Fig. 5 show an absence of upwardly sloping sublinear turn-on found in most SBMOSs [6], which is due to low Φ_{beff}. Also, there is a clear presence of linear and saturation regions for all V_g biases, indicating that the channel pinch-off has been reached.

Fig. 6 shows the I_{on}/I_{off} against L_g characteristics of GAA $ErSi_{2-x}$ N-SBNWMOSs. The I_{on}/I_{off} shows an almost constant value of ~6.5 X 10^4 for all L_g. The absolute values of I_{on} and I_{off} are independent of L_g which implies that the variations in the I_{on}/I_{off} ratio is due to the slight differences in effective Schottky barrier height (Φ_{beff}) and not due to the differences in L_g. Fig. 7 shows the I_{off}/I_{on} characteristics of the GAA $ErSi_{2-x}$ N-SBNWMOSs for various L_g values. Also included in Fig. 7 are the I_{on}/I_{off} characteristics of the best rare earth (RE) silicide SBMOS results reported [1, 8-11]. As can be seen, even at longer L_gs, the GAA $ErSi_{2-x}$ N-SBNWMOSs have comparable/larger I_{on} values.

Fig. 8 plots the SS against L_g, which shows that the SS increases slightly from ~65mV/decade to 87mV/decade as L_g decreases from 155nm to 70nm. From L_g = 155nm to 85nm, the SS increases only slightly (65mV/decade to 76mV/decade). These SS values are comparable with the lowest SS reported (70mV/decade) for an $ErSi_{1.7}$ SSDMOS with L_g = 100nm [11]. Fig. 9 plots the DIBL against L_g, which shows that the DIBL increases from around 21mV/V to 101mV/V as L_g decreases from 155nm to 70nm. From L_g = 155nm to 90nm, the DIBL increases only slightly from 21.3mV/V to 45mV/V which is close to the theoretical DIBL limit of SSDMOSs (25mV/V to 33mV/V) [11] indicating the absence of SCE.

Fig. 10 shows the temperature dependent I_d-V_g characteristics of a GAA $ErSi_{2-x}$ SBNWMOS with L_g = 90nm, measured at V_d = 50mV for a temperature range of 288K - 353K. The Schottky barrier extracted is the Φ_{beff}, taking into account both thermionic (TE) and thermionic field emission (TFE) current. It is thus is a measure of the Schottky barrier height and thickness. The associated Arrhenius plot, i.e., the plot of $\ln(I_d/T^2)$ against $1/T$ for various values of V_g was derived and shown in Fig. 11.

The corresponding extracted Φ_{beff} against V_g from V_g = -0.3V to 0.1V is shown in Fig. 12. From the slope of Fig. 12, for V_g = -0.3V to -0.15V, the current transport mechanism is dominated by TE with a slope of ~2.2eV/V. In this region, V_g modulates the Schottky barrier height towards a value ~0.32eV. At V_g = -0.15V, the Schottky barrier height is equal to 0.32eV. Beyond this value, V_g modulates the Schottky barrier thickness and TFE starts to dominate the current flow. The Φ_{beff} modulation at this point then reduces to ~1.09eV/V. Thus, the change in Φ_{beff} modulation is due to the different current conduction mechanisms. Eventually at even more positive V_g values, the Schottky barrier thickness is then effectively 'transparent' to electrons and current is limited by the SiNW resistance. This occurs at V_g = 0.03V whereby Φ_{beff} = 0.097eV.

CONCLUSION We fabricated GAA $ErSi_{2-x}$ N-SSDNWMOS with excellent electrical characteristics (I_{on}/I_{off} ratio of ~1.1 X 10^5, SS = 65mV/decade – 87mV/decade, DIBL = 21.3mV/V to 45mV/V), and with short channel performance equal to or better than reported $RESi_{2-x}$ based SBMOS. In addition, GAA PtSi P-SBNWMOSs with excellent electrical characteristics were fabricated for complementary MOSFET operation with $ErSi_{2-x}$ N-SSDNWMOS. The extracted P-SSDNWMOS characteristics are comparable or better than the currently reported PtSi P-SSDMOSs. Hence the GAA $ErSi_{2-x}$ SBNWMOS shows excellent electrical characteristics with short channel performance equal to or better than the reported $RESi_{2-x}$ based SSDMOS [1, 6, 8-11].

References

[1] J. Kedzierski *et al.*, IEDM Tech. Deg., p. 3.4.1, 2000. **[2]** N. Singh *et al.*, IEDM 2006. **[3]** K. H. Yeo *et al.*, IEDM 2006. **[4]** B. Doyle *et. al.*, ULIS 2006, p. 39. **[5]** E. J. Tan *et al.*, Ext. Abstr. SSDM 2007, p. 816. **[6]** J.M. Larson *et al.*, TED 53 p1048, 2006. **[7]** G.D.J. Smit *et al.*, APL 81 p3852, 2002. **[8]** M. Jang et al., APL 84, p. 741, 2004. **[9]** R. Lee et al., EDL 28 p. 164, 2007. **[10]** S. Zhu et al., EDL 25 p. 565, 2004. **[11]** M. Jang, J. Semicond. Tech. Sci., 6 p. 10, 2006.

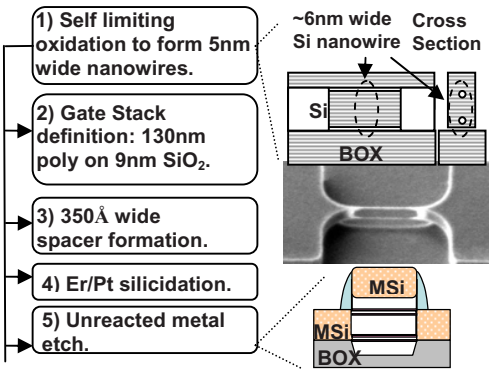

Fig. 1. Process flow of GAA SBNWMOS and schematic of device after self limiting oxidation and final device structure.

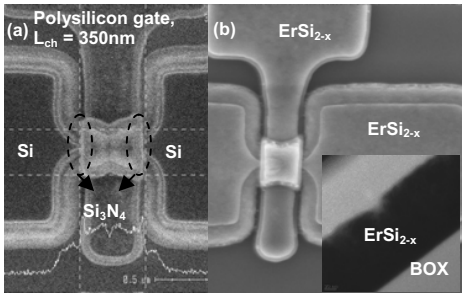

Fig. 2. (a) Top view SEM micrograph of a GAA SBNWMOS before silicidation with L_{ch} = 350nm. (b) Top view SEM of a completed GAA SBNWMOS after silicidation with L_{ch} = 350nm. Insert shows a XTEM micrograph of the fully silicided S/D pad.

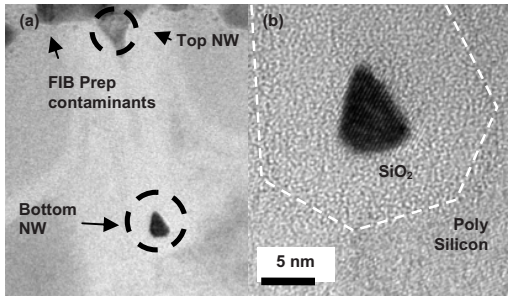

Fig. 3. (a) XTEM of a GAA SBNWMOS showing a stacked SiNW of widths ~8nm (top) and ~5nm (bottom), and (b) HRTEM of the bottom SiNW surrounded by a layer of 90Å thermally grown SiO_2 gate dielectric followed by a 1300Å layer of polysilicon.

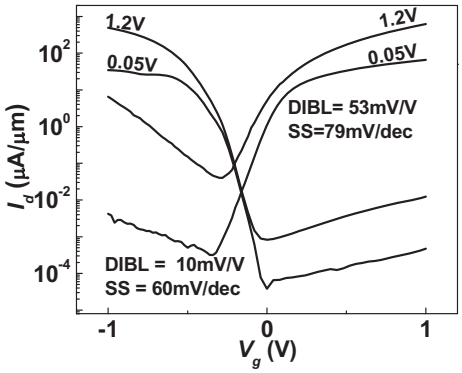

Fig. 4. I_d-V_g characteristics of the GAA $ErSi_{2-x}$ and PtSi N and P-SBNWMOS with L_{ch} = 140nm and L_g = 90nm.

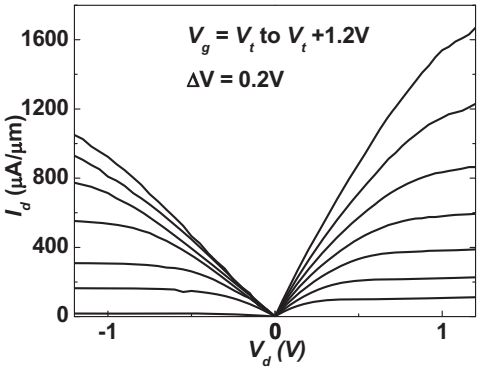

Fig. 5. I_d-V_d characteristics of the GAA $ErSi_{2-x}$ and PtSi N and P-SBNWMOS with L_{ch} = 140nm and L_g = 90nm.

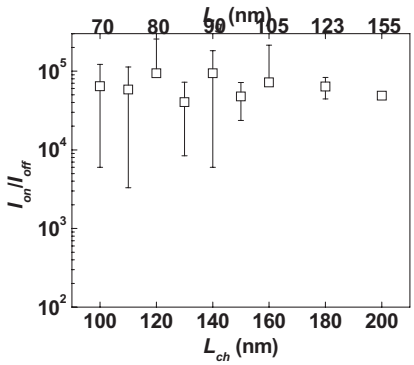

Fig. 6. Extracted I_{on}/I_{off} against L_g from 155nm – 70nm from the I_d-V_g of GAA $ErSi_{2-x}$ N-SBNWMOSs.

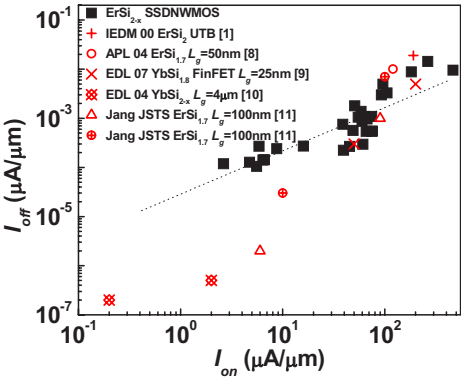

Fig. 7. Extracted I_{on}/I_{off} characteristics from the I_d-V_g of GAA $ErSi_{2-x}$ N-SBNWMOSs. I_{off} measured at V_t – 0.6V, I_{on} measured at V_t + 0.6V

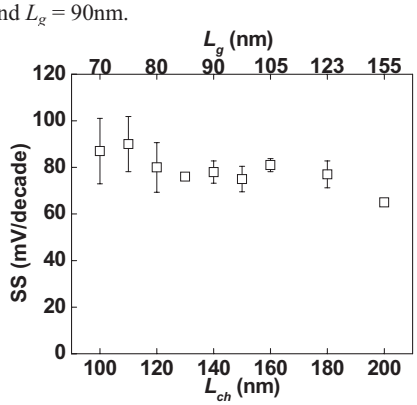

Fig. 8. Extracted SS measured at V_d = 50mV as a function of L_g from 155nm – 70nm from the I_d-V_g of GAA $ErSi_{2-x}$ N-SSDNWMOSs.

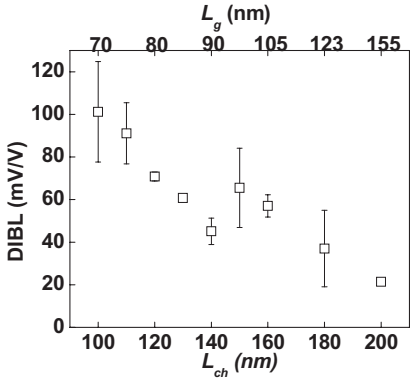

Fig. 9. Extracted DIBL as a function of L_g from 155nm – 70nm from the I_d-V_g of GAA $ErSi_{2-x}$ N-SSDNWMOSs.

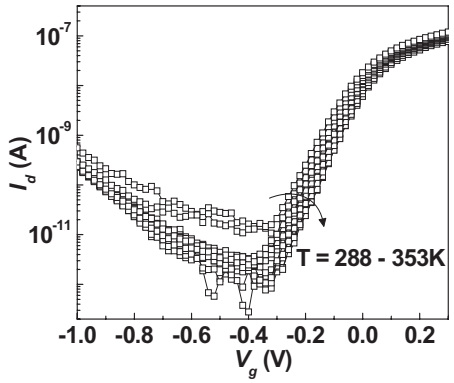

Fig. 10 Temperature dependent (288K to 353K) I_d-V_g measured at V_d = 50mV.

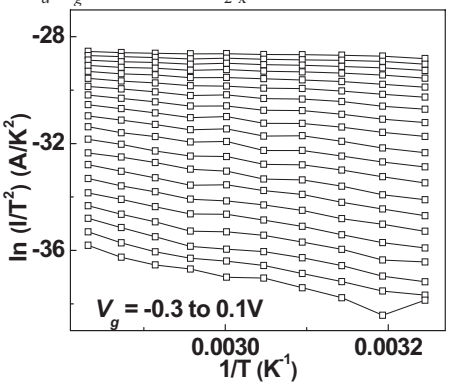

Fig. 11. Arrhenius plot, i.e., plot of $\ln(I_d/T^2)$ against $1/T$ for various values of V_g.

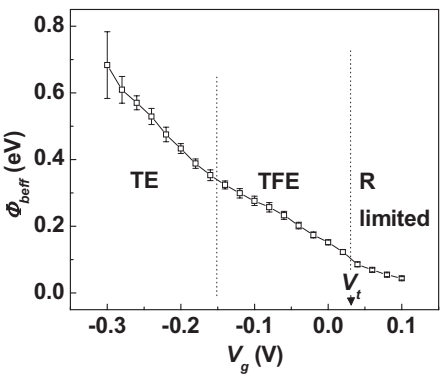

Fig. 12. Φ_{beff} against V_g. The error bars indicate fitting errors.