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Principal Guideline of Stress Design Engineering for Drivability Enhancement and Suppression of Variability in PMOSFET with SiGe S/D

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Abstract

We have developed the guideline for stress design engineering with embedded Silicon Germanium (eSiGe) source drain (S/D) technology. It enables us to improve drivability and to suppress the variety in Vth. Based on this guideline, the minimization of Si loss above extension region is performed not only to improve drivability enhancement but also to suppress variation in Vth in PMOSFET due to suppression of dislocations which are generated at channel edges. This technique controls stress discontinuity at channel edge, hence enables us to use our new high Ge-mole-fraction profile to enhance the mobility. Furthermore, by optimization of MSA temperature, we successfully avoided stress relaxation of eSiGe even in high Ge-mole-fraction condition. Consequently, this stress technique realized a 19.2 % improvement in Ion for Ioff = 100 [nA/μm] at Vd = 1.0 [V], and Ion = 809 [μA/μm] was successfully achieved, while variety in Vth was kept as low as reference with box Ge profile. We also demonstrate that this scheme was compatible with NMOSFETs.

I. Introduction

Recently, the demand for stress design in scaled CMOSFETs is increasing because process-induced strain technology has become standard, such as dual stress liner (DSL) technique[1], and eSiGe S/D technology[2] for improvement of electrical performance in scaled CMOSFETs. For example, DSL technique causes layout dependence for such as layout boundary, stacked layout, contact hole pitch and so on. These effects come from differences of their volumes in various layouts[3-6]. It is pointed out the suppression of such boundary dependences is important from the point of view on device design[7, 8]. We focused on eSiGe technique which is widely used as the booster for PMOSFETs. As indicated below, this is our guideline for stress design on eSiGe. First, increasing stress to the channel for enhancement of mobility without relaxation eSiGe itself. In addition, for the dislocation formation suppression at channel edges, stress profile by eSiGe must be smooth since the abrupt stress profile causes the penetration from eSiGe near the channel. Finally, it is necessary to optimize MSA temperature to keep eSiGe with high Ge mole fraction from stress relaxation.

In this paper, we describe stress design scheme aiming at both improvement of the device performance and the suppression of variability in PMOSFETS. Moreover, we show that this scheme has compatibility to NMOSFETs characteristics.

II. Device Concept

To achieve the mobility enhancement for high performance PMOSFETs, the easiest solution is increasing Ge mole fraction in eSiGe layer. However, it is difficult to increase its stress for the device without exceeding the critical thickness[9], which is given by Ge mole fraction. That is to say, it causes stacking fault results in degraded device performance. To overcome this problem, we applied high Ge mole fraction SiGe layer for only adjacency to the channel. On the other hand, it is also necessary to keep its strong stress without stress relaxation by dislocation formation at Si channel. For this requirement, we speculate that minimization of Si loss above extension region is the very key process since stress gradient becomes abrupt by the stressors around this unintentional regions. These dislocations come from two stressors, One is the spacer which has compressive stress in vertical direction to the channel, the other is eSiGe applying compressive stress in horizontal direction to the channel. Both stress relaxation and dislocation formation cause not only degradation of device performance but also increase in the variability of device. Furthermore, after stressor and structural optimization, it is necessary to fine tune the millisecond annealing (MSA) temperature. That is to say, MSA applying high temperature such as laser-spike annealing (LSA) and flash lamp annealing (FLA) has more severe drawback for stress relaxation on high Ge mole fraction SiGe than that on conventional Ge mole fraction SiGe.

Figure 1 summarizes preceding discussion with schematics on 45-nm-node PMOS with Σ-shaped eSiGe source drain[10-13]. Left side in Figure 1 describes problems using high Ge mole fraction for eSiGe. Right side summarizes the concept of solutions as mentioned before.

III. Result and Discussion

I. Optimization of Ge profile in eSiGe

Figure 2 shows the cross-sectional TEM micrographs of our pMOSFET with Σ-shaped eSiGe S/D incorporated both high Ge mole fraction layer and buffer layer (a), and (b) is close-up of Σ-shaped eSiGe S/D. It is seen that two layers with different contrast in TEM image, that is, lower Ge mole fraction layer as buffer layer. As mentioned above, the key process is optimization of Ge profile in these two layers[14]. On the other hand, in figure 2 (c), it is observed stacking fault is heavily penetrating in eSiGe in case of graded Ge mole fraction layer as buffer layer. Abrupt Ge profile seems more effective for suppression of dislocation formation than graded Ge mole fraction layer. This difference comes from abrupt Ge mole fraction profile enable us to pin dislocation in high Ge mole fraction region due to forming 60º dipole[15]. Thus, we optimized abrupt Ge profile in order to confine dislocations even in device structures. Figure 3 shows comparison of Vth-rolloff characteristics among with and without optimized Ge profile, and box Ge profile as reference. It is noted that device with relaxed eSiGe has deeper roll-off curve because of lower stress than that of both reference with box Ge profile and optimized Ge profile devices. Using optimized high Ge mole fraction profile can actually improve both the Ion and the Idlin of 45-nm-node PMOS by 5.6% and 9.7% at Ioff = 100 [nA/μm] resulted from the mobility enhancement without stress relaxation (figure 4 (a), (b)) for the same Vth-rolloff characteristics (Figure 3). In order to confirm the mechanism, we measured Rtotal as a function of gate lengths (Figure 5). Shallow slopes of total device resistance for optimized Ge profile indicate enhanced mobility. Significant improvement (13.8 %) is achieved in optimized Ge profile with high Ge mole fraction. However, variation in Vth is slightly deteriorated by using high Ge mole fraction profile due to relaxation of strain occurred in random, even if Ge profile is well optimized (Figure 6).

II. Minimization of Si loss above SD extension region

Figure 7 shows mechanism of stress transfer and how Si loss affects device performance in our pMOSFET. In TEM image (Inset of figure 7) , it is observed that stacking fault is heavily penetrating at channel edge. This dislocations resulted in increasing the variability by random stress relaxation, as shown in figure 6. In order to clarify this mechanism, we simulated 1D strain (εxx, εyy) distribution in pMOSFETs with eSiGe S/D (Figure 8). It is found that substrate recess in SD extension regions makes strain gradients dramatically discontinuous. This result indicates that undesirable dislocations are formed at channel edges, where the stress distribution is complicated (as mentioned in chap. II). Therefore, we applied Si loss minimization technique to resolve this serious issue. Consequently, owing to the reduction of Rtotal, which is associated with extension resistance, by 57 [Ω-μm], the Ion of 45-nm-node PMOS is drastically improved by 9.4% at Ioff = 100 [nA/μm] resulted from not only reduction of parasitic resistance but also from dislocation formation suppression at channel edges by eSiGe with high Ge mole fraction [12,13], as shown in Figure 9. The Vth-rolloff characteristics with and without this technique are comparable (Figure 10). By removal of discontinuity in strain slope, variation in Vth was controlled to be comparable to box Ge profile (Figure 11). This means strain discontinuity around substrate recess is a source of Vth fluctuation resulted from dislocation at channel edges.

III. Optimization of MSA temperature for high Ge conc. SiGe

MSA temperature for PMOSFETs with suppression of SiGe relaxation have been intensively studied by many researchers [16-18]. We found that the lower MSA temperature has much advantage to suppression of relaxation even for high Ge mole fraction profile in PMOSFETs. Moreover, this range of MSA temperature has no disadvantage for NMOSFETs. Using optimized MSA temperature can actually improve the Ion of 45-nm-node PMOS by 4.3% improvement at Ioff = 100[nA/μm] resulted from suppression of stress relaxation with our high Ge-mole-fraction profile for the same Vth-rolloff characteristics (Figure 12, 13). As described above, by using this technique, we also obtained Vth-rolloff and Ion-Ioff of NMOSFETs are comparable to conventional temperature (Figure 14). This means that NMOSFETs are insensitive for our MSA temperature, however PMOSFETs with high Ge mole fraction eSiGe are still sensitive for MSA temperature. Furthermore, this scheme is compatible to advanced junction profile design scheme reported in reference [16, 18].

Figure 15 shows the summary of device performance in this work. Ion = 809 [μA/μm] for Ioff=100 [nA/μm] at Vdd = 1.0 V was successfully achieved. And, variety in Vth is almost same as reference with box Ge profile (Figure 11).

IV. Conclusion

We have demonstrated the strategic guideline for stress design engineering focusing on eSiGe S/D technology, which consists of three techniques. We successfully controlled stacking faults and dislocations simultaneously both in eSiGe and Si channel edges. Consequently, a 19.2 % improvement in Ion for Ioff = 100 [nA/μm] at Vd = 1.0 [V], and Ion = 809 [μA/μm] was successfully obtained by these stress techniques which was compatible with NMOSFETs.

Reference

[1] H. Yang et al., IEDM Tech. Dig, pp. 1075, 2004. [2] T. Ghani et al., IEDM Tech. Dig., pp. 987, 2003.[3] P. Grudowski et al., Symp. VLSI Tech. Dig, pp. 62, 2006. [4] T. Miyashita et al., Ext. Abst. SSDM, pp. 170, 2006. [5] R. Liebmann et al., SISPAD, pp. 173, 2006. [6] S. Cea, et al., IEDM Tech. Dig, pp. 963, 2004. [7] A. Oishi et al., IEDM Tech. Dig., pp.229, 2005.[8] M. Nishikawa et al., Ext. Abst. SSDM, pp. 868, 2006. [9] D. C.Houghton et al., J. Appl. Phys. **70**, pp.2115, 1991. [10] H. Ohta et al., IEDM Tech. Dig., pp.247, 2005. [11] N. Tamura et al., IWJT Conf. Proc., pp. 73, 2008. [12] Y. Shimamune et al., VLSI Tech., pp. 116, 2007. [13] Y. S. Kim et al., IEDM Tech. Dig., pp.871, 2006. [14] J. –P. Han et al., IEDM Tech. Dig., pp. 59, 2006. [15] C. –X. Li et al., Superlatt. Microstruct. **40**, pp. 113 ,2006. [16] T. Yamamoto et al., IEDM Tech. Dig., pp. 143, 2007. [17] T. Sanuki et al., IEDM Tech. Dig., pp. 281, 2007. [18] K. Ikeda et al., VLSI Tech., pp. 188, 2008.

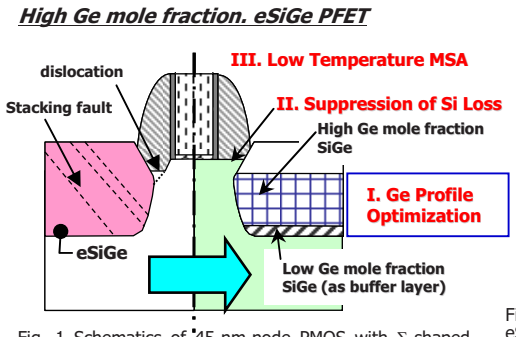


Fig. 1 Schematics of 45-nm-node PMOS with Σ-shaped high Ge mole fraction eSiGe S/D. Left side shows problems using high Ge mole fraction for eSiGe. Right side shows the concept of our solutions.

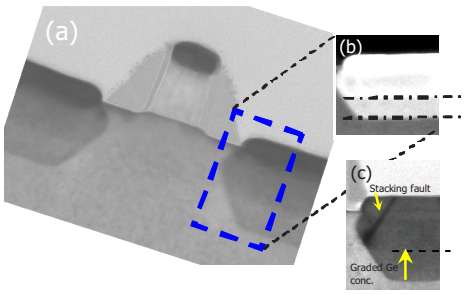


Fig. 2 Cross-sectional TEM images of pFET with Σ-shaped eSiGe S/D[10-13] with high Ge mole fraction layer and buffer layer (a), and the inset (b) is closeup of Σ-shaped eSiGe S/D. (c) shows example of stacking fault in case of graded Ge mole fraction layer as buffer layer.

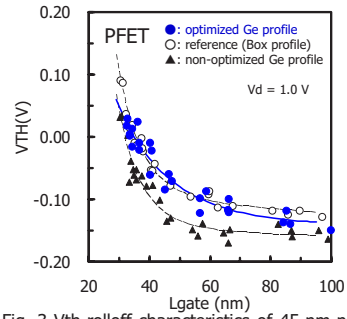


Fig. 3 Vth-rolloff characteristics of 45-nm-node high-performance PMOS with non-optimized high Ge mole fraction profile (solid triangle), with (solid circle) and without optimized Ge profiles (open circle).

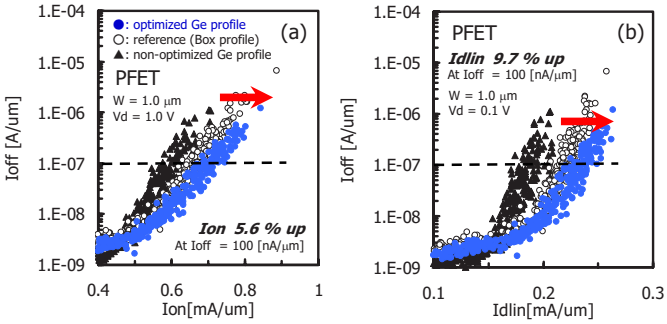


Fig. 4 Ion-Ioff (a) and Idlinl-Ioff (b) characteristics of 45-nm-node PMOS with and without optimized buffer layer. An 5.6% improvement in saturation on-current (Ion) at Ioff = 100 [nA/μm] resulted from the enhancement of mobility by SiGe with high mole fraction Ge profile without relaxation of strain.

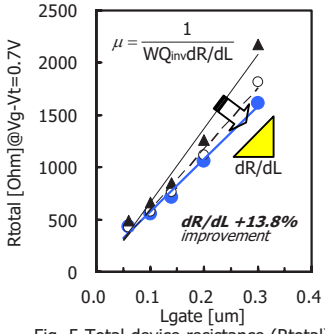


Fig. 5 Total device resistance (Rtotal) as a function of gate lengths. eSiGe with optimized high mole fraction Ge profile effectively enhanced mobility.

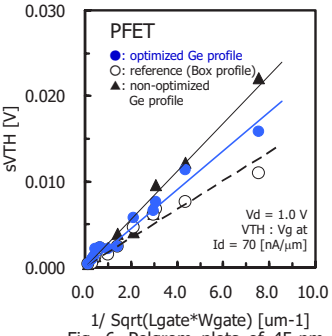


Fig. 6 Pelgrom plots of 45-nm node high performance PMOS with and without optimized Ge profiles in eSiGe S/D.

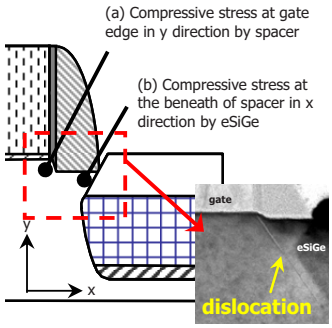


Fig. 7 Schematic of mechanism of stress transfer, how Si loss (extension recess) affects device performance. Inset shows TEM image of dislocation at channel edge

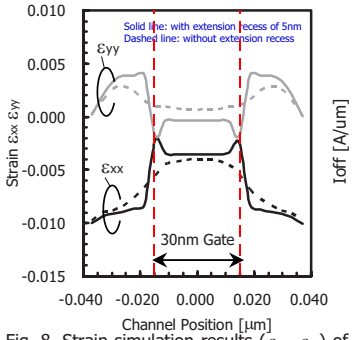


Fig. 8 Strain simulation results (ε_{xx}, ε_{yy}) of pMOSFET. Substrate recess (solid line) seems to make gradients dramatically discontinuous. ε_{xx} means longitudinal strain, ε_{yy} for vertical strain to the channel.

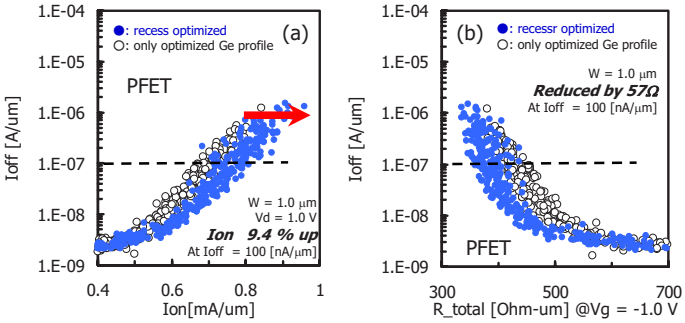


Fig. 9 Ion-Ioff (a) and Rtotal-Ioff (b) characteristics of 45-nm-node PMOS with optimization of stress transfer. A 9.4% improvement in saturation on-current (Ion) at Ioff = 100 [nA/μm] resulted from not only reduction of parasitic resistance but also suppression of dislocations at channel edge by eSiGe with high Ge mole fraction.

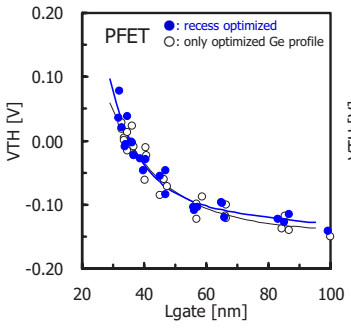


Fig. 10 Vth-rolloff characteristics of 45-nm-node high-performance PMOS, with (solid circle) and without (open circle) minimization of Si loss above extension region.

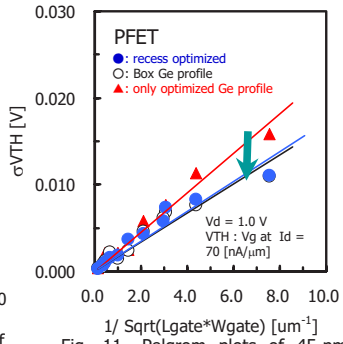


Fig. 11 Pelgrom plots of 45-nm node high performance PMOS with (solid circle) and without (solid circle) minimization of Si loss.

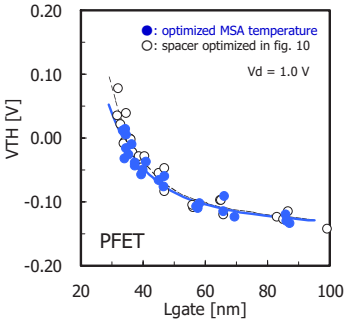


Fig. 12 Vth-rolloff characteristics of 45-nm-node high-performance PMOS, with (solid circle) and without (solid triangle) optimization of MSA temperature which is compatible with NMOSFETs.

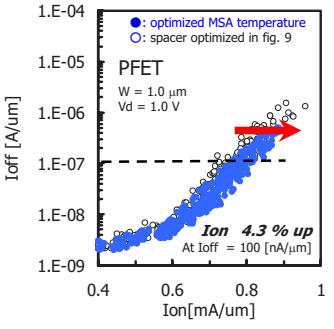
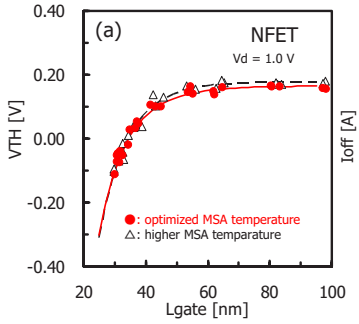


Fig. 13 Ion-Ioff characteristics of 45-nm-node high-performance PMOS, with (solid circle) and without (open circle) optimization of MSA temperature.



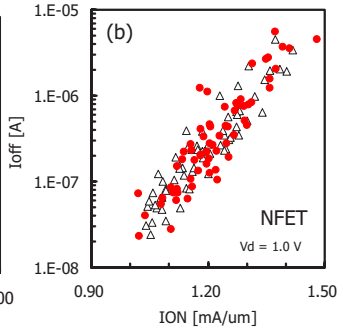


Fig. 14 Vth-rolloff (a) and Ion-Ioff (b) characteristics of 45-nm-node high-performance NMOS, with (solid circle) and without (open triangle) optimization of MSA temperature which is compatible with PMOSFETs (Fig. 13).

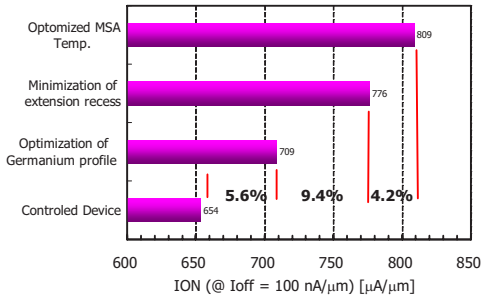


Fig. 15 Summary of device performance in this work.