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Design and Optimization of Gate Sidewall Spacers to Achieve 45nm Ground Rule for High-performance Applications

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Introduction

When the technology node advances to the next generation, one of the biggest challenges is to achieve 0.7x minimum pitch while maintaining device performance. In such a situation, the design of gate sidewall spacers and their integration into the CMOS fabrication flow while maintaining good compatibility with other booster technologies, are particularly important because the width of sidewall spacer can not be simply scaled without deteriorating short channel immunity. Moreover, the material of the sidewall spacer itself plays an important role, and its impact on device performance has been intensively discussed from the viewpoints of parasitic capacitance [1-3], parasitic resistance reduction [4,5], metal/high-*k* gate stack specific issues [6], and the modulation of channel strain [7,8]. However, there have been few reports on the gate sidewall spacer design for 45nm technology node considering the structure and material. In this paper, we developed a triple sidewall spacer scheme and optimized it to achieve 45nm ground rule. We also discuss the impact of spacer material on device performance improvement.

Triple Sidewall Spacer Scheme

Fig. 1 shows the process sequence and the schematic diagram of the gate X-section. We used a triple sidewall spacer scheme of source/drain extension (SDE) implantation offset (SW1), embedded-SiGe (eSiGe) offset (SW2), and deep source/drain (SD) implantation offset (SW3), combined with in-situ doped eSiGe technology which is inserted after SDE formation. After the gate stack etching, SW1 was firstly formed by the deposition and etch-back processes, followed by halo and SDE implantations. Then SW2 was formed and buffer implantation was performed for reducing parasitic resistance and silicide junction leakage. After the SiGe module was completed, SW3 was formed for the offset of the following deep SD implantation. Note that SW3 was stripped just before the silicidation process.

Results and Discussion

(a) SW1 for SDE ion implantation offset

The offset spacer for SDE ion implantation is widely used in high-performance CMOS technology. Because the impurity profiles of the SDE tip directly affect the short channel characteristics, simultaneous optimization of SW1 and SDE implantation is indispensable for enhanced performance. Fig. 2 shows the dependence of the NFET I_{on}-I_{off} relationship on SW1 materials. Note that the device with SiO_2-SW1 was implanted with a 10% higher SDE dose. Although offset widths for different SW1 materials were almost the same, I_{on}-I_{off} characteristics were severely degraded for the case with SiO_2-SW1. In addition, a difference in drive current was also observed for the devices with Si_3N_4-SW1 depending on the source gas during deposition. The main cause of these results is the difference in parasitic resistance. Fig. 3 shows the parasitic resistance, R_{para} and SDE sheet resistance, R_{ext} for different SW1 materials. The R_{para} indicates good correlation with drive current, and the highest R_{para} for the device with SiO_2-SW1 is due to the diffusion of SDE arsenic (As) into the spacer. As a consequence, the impurity profile at the SDE tip was modulated and the resistance in this region was increased. This phenomenon is also observed for PFET with boron (B) SDE, although its impact is smaller than NFET. Reliability issues were confirmed by PFET NBTI as shown in Fig. 4(a), and the impact of spacer materials was almost negligible. We also confirmed negligible impact on NFET HC lifetime by using 1.8V I/O transistors (Fig. 4(b)).

(b) SW2 for PFET eSiGe offset

As we have previously described, SW2 acts as an offset to control the proximity of eSiGe to the channel. We can enhance the channel strain by using close proximity of eSiGe [9,10], however, it also deteriorates the threshold voltage, V_{th} roll-off characteristics in the case of using in-situ doped SiGe. Fig. 5 shows the dependence of V_{th} on L_g for different SW2 deposition thicknesses. It is clearly seen that the decrease in SW2 deposition thickness results in degraded PFET roll-off characteristics, while NFET roll-off curves indicate almost no sensitivity to the SW2 thickness. This is mainly due to the B diffusion from SiGe:B in the SD regions, and it is important to design the distance between the channel and eSiGe by controlling the offset width of the SW2. The structure of SW2 also affects the device characteristics. Fig. 6 shows the TEM X-section of NFETs with both Si_3N_4/SiO_2 stack and Si_3N_4 only SW2 structures. The drive current dependence on SiO_2 thickness in the Si_3N_4/SiO_2 stacked structure for NFET is shown in Fig. 7. As can be seen in this figure, the drive current is improved with the decrease in SiO_2 thickness, while keeping the V_{th} roll-off characteristics unchanged. This result confirms that the diffusion of extension As into SW2-SiO_2 was suppressed similar to the case in SW1. One of the concerns in eliminating SW2-SiO_2 is the increase in parasitic capacitance, especially in gate to contact capacitance; however, its impact is less than 5% even at the minimum gate to contact space as shown in Fig. 8.

In addition to the SW2 structure, the selection of spacer material is another key factor for performance enhancement. We investigated the impact of SW2-Si_3N_4 films on device characteristics especially focusing on PFET. Because the SD recess is formed through SW2 as an offset mask, Si_3N_4 should be used as the SW2 in our process with low dry and wet etch rates. Fig. 9 shows the PFET R_{ext} under the same implantation conditions for different SW2-Si_3N_4 materials. It is found that the R_{ext} under low-temperature *Si_3N_4-3* [8] SW2 is 35% higher than that under *Si_3N_4-1* SW2. This can be explained by SIMS profiles of SDE B as shown in Fig. 10. It is clear that the B impurities under *Si_3N_4-1* SW2 diffused much more than those under low and high-temperature *Si_3N_4-3* SW2, and the relative integrated B dose of between 10^{18} and 10^{20} cm^{-3}, which mainly contributes to R_{ext}, is larger for the case with *Si_3N_4-1* SW2 as shown in the inset. This enhanced B diffusion is attributed to the remaining Si-H bonds in *Si_3N_4-1* film. Because the Si-H bond is unstable and the hydrogen atoms can be easily released, the diffusion of SDE B was much more enhanced with the hydrogen assist. Figs. 11 and 12 show the PFET device characteristics with different SW2-Si_3N_4 materials. In these figures, both the SDE B implantation energy and dose are 30% higher for the case with *Si_3N_4-3* SW2. Even with the higher energy and dose condition, the device with *Si_3N_4-3* SW2 shows improved roll-off characteristics and corresponding degraded drive current. However, they have a trade-off relationship and we can select whichever material we want taking into account the productivity and cost.

(c) SW3 for NFET deep SD ion implantation offset

As ions are commonly used for NFET deep SD implantation, however, the use of phosphorous (P) instead of As is very attractive due to its higher solubility and the resultant lower SD resistance and thinner effective oxide thickness. We have introduced SW3 in order to use P as a deep SD impurity; the design of SW3 is shown in Fig. 13. Of course, it becomes increasingly difficult to maintain a larger offset for ion implantation when the poly pitch shrinks, therefore we formed SW3 only for NFET deep SD implantation and it was completely stripped just before the silicidation process. The non-contacted minimum poly pitch in our technology is 140 nm. Although the poly to poly space in such a small pitch is filled with SW3 as schematically shown in Fig. 13 when the offset width is optimized in order not to affect the short channel behavior, the silicide characteristics are hardly affected because buffer implantation has been carried out through SW2 as shown in Fig. 1. Fig. 14 shows the SEM X-section of NFET after the formation of SW2 and SW3 for two different poly pitches. In the case of the 140-nm-pitch device, it can be seen that the poly to poly space is filled with SW3, whereas there exists open space for the device with the contacted minimum pitch (180 nm). As shown in Fig. 17, the silicide sheet resistance at the minimum contacted poly pitch is an acceptable value, and is tolerant to fluctuations in SW2 width. Moreover, the increase in NFET junction leakage current with minimum non-contacted poly pitch (corresponding to the case without deep SD implantation) compared with the case of large poly pitch was suppressed to less than one order of magnitude (Fig. 18), and so we can achieve 45nm node pitch with this triple sidewall spacer scheme.

Finally, the device characteristics of the three stacked poly layout with minimum contacted pitch are shown in Figs. 19 and 20 for N- and PFET, respectively. In these figures, both the V_{th} and I_{on} dependences on L_g of an isolated device are also shown for comparison. Although variation of L_g depending on the gate position is observed due to non-optimized OPC in gate lithography, almost identical device characteristics were obtained even in the minimum pitch layout. Therefore, we conclude that our sidewall spacer design is mature and suitable for 45nm technology.

Conclusion

We have developed a triple sidewall spacer scheme, in which SW1 is used for SDE implantation offset, SW2 for PFET eSiGe offset, and SW3 for NFET deep SD implantation offset. We also discussed the impact of sidewall spacer materials on device characteristics. After optimizing the spacer width and material, we have successfully demonstrated identical device characteristics with the minimum poly pitch layout while minimizing the dependence on layout.

References

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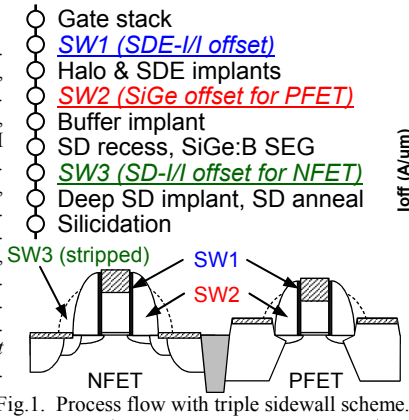

Fig.1. Process flow with triple sidewall scheme.

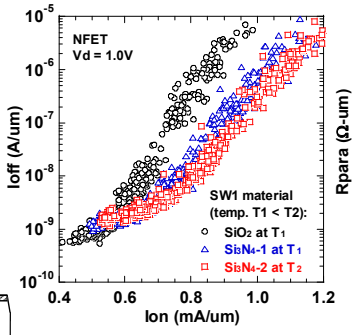

Fig.2. Comparison of NFET I_{on}-I_{off} characteristics for different SW1 materials.

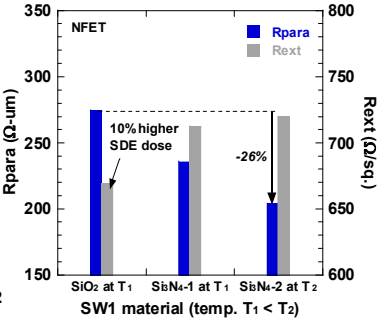

Fig.3. Comparison of NFET R_{para} and R_{ext} for different SW1 materials.

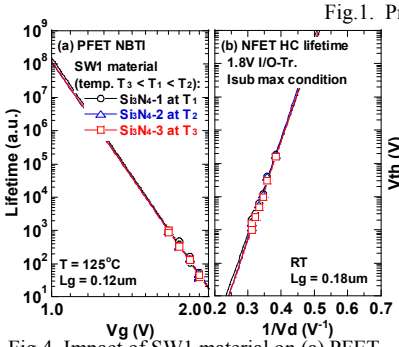

Fig.4. Impact of SW1 material on (a) PFET NBTI and (b) NFET HC lifetime.

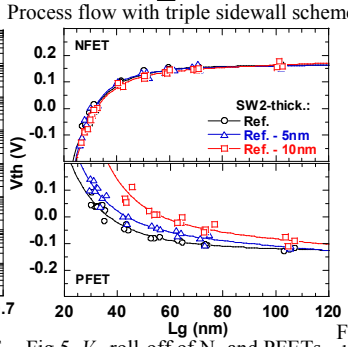

Fig.5. V_{th} roll-off of N- and PFETs with different SW2 deposition thickness.

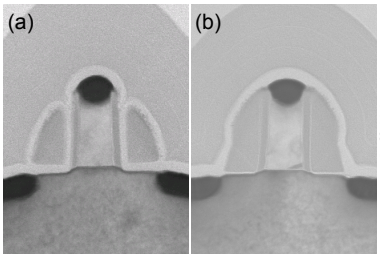

Fig.6. TEM cross-section of NFETs with different SW2 structures. (a) Si_3N_4/SiO_2 stack and (b) Si_3N_4-only structures, respectively.

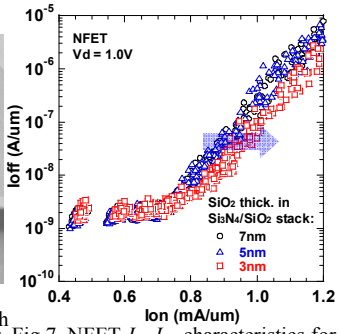

Fig.7. NFET I_{on}-I_{off} characteristics for different SiO_2 thickness in SW2 stack.

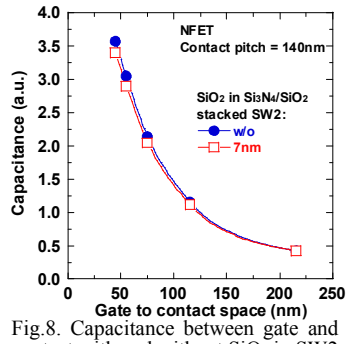

Fig.8. Capacitance between gate and contact with and without SiO_2 in SW2 stack.

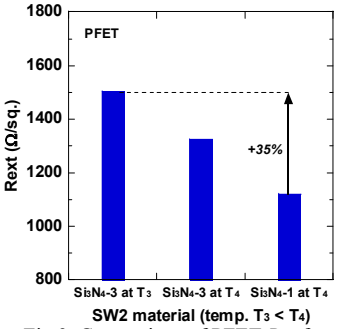

Fig.9. Comparison of PFET R_{ext} for different SW2-Si_3N_4 materials.

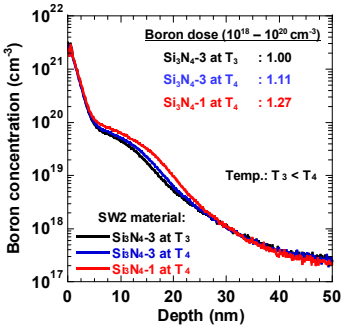

Fig.10. SIMS profiles of PFET SDE for different SW2-Si_3N_4 materials.

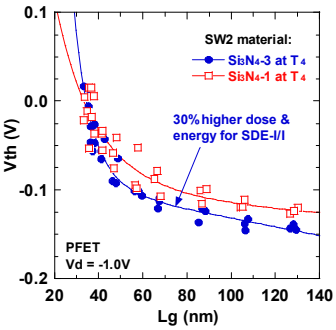

Fig.11. Comparison of PFET V_{th} roll-off for different SW2-Si_3N_4 materials.

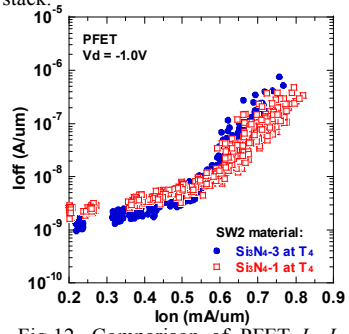

Fig.12. Comparison of PFET I_{on}-I_{off} characteristics for different SW2-Si_3N_4 materials.

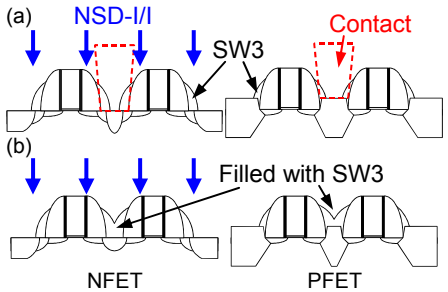

Fig.13. Schematic diagram of SW3 design to achieve minimum (a) contacted and (b) non-contacted poly pitch.

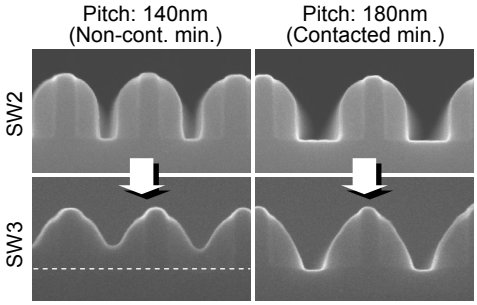

Fig.14. SEM cross-section of NFET after SW2 and SW3 formation for two different poly pitches (140/180nm).

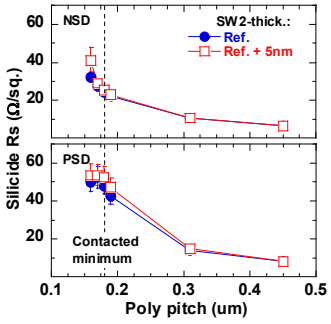

Fig.15. Poly bounded silicide sheet resistance as a function of poly pitch.

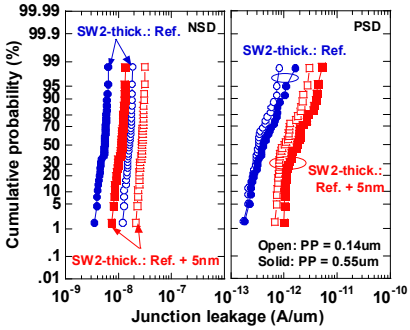

Fig.16. Distribution of poly bounded silicide junction for minimum and large poly pitch.

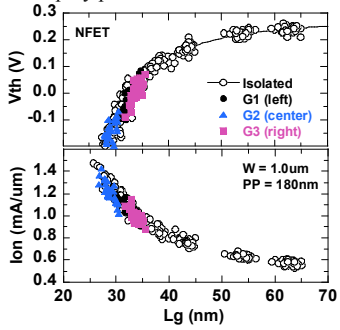

Fig.17. NFET V_{th} and I_{on} vs. L_g for three-stacked layout with min. contacted poly pitch.

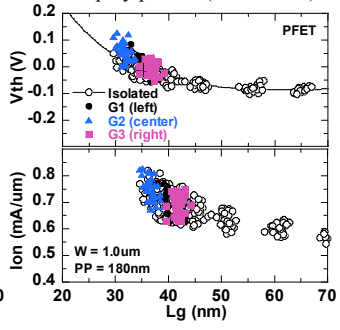

Fig.18. PFET V_{th} and I_{on} vs. L_g for three-stacked layout with min. contacted poly pitch.