Hot-Carrier AC Lifetime Enhancement due to Wire Resistance Effect (WRE) in 45nm CMOS Circuits

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1. Introduction
Hot-carrier injection (HCI) has been one of the major concerns on VLSI reliability issues. The gate length reduction while keeping the supply voltage around 1-V results in the serious HCI degradation of advanced 45nm CMOS devices. According to our estimation, the lifetime of discrete device is reduced by almost an order of magnitude for the next process generation.

This paper describes the HCI AC lifetime enhancement phenomenon in 45nm CMOS circuits, thanks to the following new factors.
(1) The worst gate voltage of HCI degradation has been changed.
(2) Large wire resistance plays a shield role in load capacitance.
So delay degradation was found to be less than half in this WRE (wire resistance effect).

2. Analysis method
Figure 1 shows the measured HCI lifetime of acceleration test for both 1.0V and 1.8V devices, as a function of Vgs (gate-voltage). The test condition of Vds (drain-voltage) is 1.8V for 1.0V device, and 3.4V for 1.8V device. It is known that the worst HCI condition for Vgs is around half-vdd (supply voltage) [1] like the 1.8V device (referred to as submicron device). However, the lifetime of the 1.0V device (referred to as sub-100nm device) decreases as the stressing Vgs increases. To evaluate the influence of this difference on SoC logic design, the circuit degradation was simulated by using our in-house HCI simulator [2] along with the two models modified from the 1.0V device: the submicron device model and the sub-100nm device model.

Figure 2 shows the circuit structure used in the simulation. Ten inverters are connected in series. The RC effect of the wires between inverters has been newly considered. The π/4-model in Fig.2 is used for the wire as a function of the length. When the fanout is larger than 1, the wires are branched at the inverter output. To make the simulation results clear, HCI degradation model is applied only to the middle inverter, INV06, while other nine inverters are assumed not to degrade and are used just for waveform shaping. A 100-MHz clock is input continuously for 10 years, resulting in the HC degradation of INV06. The delays from Nin5 to Nin7 (one-buffer delay) are compared between before and after the stress clock. The ratio of the difference to the original delay is defined as ∆tpd%. It has been shown that the transition slope is the key factor which determines the ∆tpd% [3]. The dependence of ∆tpd% on the transition slope is examined by changing the wire length. The wire length is different between RCin and RCout in Fig.2, so that the input and output transitions of INV06 can be controlled independently.

3. Simulation results and discussions
Figure 3 shows the results for the submicron device model. The ∆tpd% dependence both on input transition (rise) of INV06 (Nin6) and on output transition (fall) at the end of the wire (the input of INV07 (Nin7)) is mapped. The fanout is equal to 1. The worst ∆tpd% occurs when both input transition (rise) at Nin6 and output transition (fall) at Nin7 are large. This is consistent with the previous results [3]. The slow input transition keeps the Vds at nearly vdd for a long time. These are the worst Vgs and Vds conditions...
for the submicron device. And the wire resistance has little impact on the $\Delta t_{pd\%}$.

Figure 4 shows the $\Delta t_{pd\%}$ for the sub-100nm technology model. As shown in Fig.4 (a), the worst condition moves to the small input transitions at Nin6 with large output transitions at Nin7. The $\Delta t_{pd\%}$ is almost double of that for the submicron device. These changes of Fig.4(a) from Fig.3 can be explained by the lifetime dependence on $V_{gs}$. The steep input transition with the slow output transition sets the main stress condition at high $V_{gs}$ and high $V_{ds}$, which is the worst for the sub-100nm device. Interestingly, as shown in Fig.4 (b), the worst $\Delta t_{pd\%}$ is reduced by half when the wire resistance is taken into account. Although the worst lifetime of the sub-100nm technology is far less than that of the submicron model, the worst $\Delta t_{pd\%}$ is almost the same as shown in Fig. 3 (b) and Fig. 4 (b).

The reason why the worst $\Delta t_{pd\%}$ for sub-100nm device model is reduced by considering the wire resistance is as follows. Figure 5 shows the simulated waveform of the output of INV06 before the wire, Nout6, along with the input, Nin6. The input transition is sharp while the output transition is slow, which is the worst condition for sub-100nm devices. Fast voltage drop is observed only for with wire resistance (w.wire-R). This comes from the capacitance shielding by the wire resistance. The fast voltage drop improves the lifetime greatly, because the lifetime exponentially depends on $1/V_{ds}$. The 100mV reduction of $V_{ds}$ could improve the lifetime by an order of magnitude. On the other hand, the submicron model has shown no improvement by considering the wire resistance. This is because the degradation mainly occurs at half-$vdd$ where the output voltage still stays at $vdd$. The wire resistance has no influence at this period.

The situation is different when the fanout is large. Table 1 shows the dependence of $\Delta t_{pd\%}$ on the number of fanout. The results are for small input transitions at Nin6 with large output transitions at Nin7. When the fanout is large, the WRE disappears. This is because each wire length is shorter for the larger fanout under the same output transition. This makes the wire resistance smaller, attenuating the capacitance shielding.

4. Conclusions
It has been shown that the HC lifetime constraint can be alleviated for 45nm devices, which have the worst condition at $V_{gs}$ of $vdd$. This is due to the capacitance shielding effect of the wire resistance. However, additional design constraint regarding the number of fanout is required when the capacitance shielding effect is weakened.

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References

Table I HCI degradation ($\Delta t_{pd}$)10years later

<table>
<thead>
<tr>
<th>Fanout</th>
<th>F.O.1</th>
<th>F.O.8</th>
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<tbody>
<tr>
<td>(a) without wire resistance</td>
<td>9.3%</td>
<td>9.2%</td>
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<tr>
<td>(b) with wire resistance</td>
<td>3.7%</td>
<td>8.8%</td>
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