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High Mobility SiGe Channel pMOSFETs Epitaxially Grown on Si (100) Substrates with $HfSiO_2$ High-k Dielectric and Metal Gate

Jungwoo Oh, Prashant Majhi, Chang Yong Kang, and Raj Jammy
SEMATECH, 2706 Montopolis Drive, Austin TX 78741, USA

Raymond Joe, Takuya Sugawara, Yasushi Akasaka, Takanobu Kaitsuka, Tsunetoshi Arikado, and Masayuki Tomoyasu
Tokyo Electron Ltd.

Introduction

Recently, high mobility pMOSFETs were demonstrated on strained or relaxed SiGe-on-Si heterostructures [1-2] with Si cap/SiGe channel quantum well structures. In this work, without using Si cap process, we have fabricated high performance SiGe channel pMOSFETs after optimizing epitaxial SiGe-on-Si and high-k dielectric/metal gate process. High mobility with low off-state current have been achieved and correlated with epitaxial SiGe-on-Si processes.

Device Fabrication

Epitaxial SiGe films were selectively grown on shallow trench isolation formed Si (100) substrates. Varying Ge concentrations (25% and 40%) of epi-SiGe channels were optimized with excellent wafer uniformity. Atomic layer deposition (ALD) $HfSiO_2$ gate dielectrics were deposited on undoped epi-SiGe channels after surface passivation, followed by sputtering of appropriate metal gates. Fig. 1 shows TEM images of pMOSFETs with a high-k $HfSiO_2$ gate dielectric/metal gate deposited on epi-SiGe channel. $HfSiO_2$ remained amorphous with a little SiO_2 interfacial layer.

Results and Discussion

Fig. 2 compares C-V curves of SiGe MOS capacitors (25% and 40% Ge). EOT of 13.6 Å and 14.0 Å were extracted using CVC model from 25% and 40% Ge capacitors, respectively. The physical thickness of $HfSiO_2$ is 40 Å. Minimal C-V hysteresis at 1 MHz was measured to be <10 mV (25% Ge) and ~20 mV (40% Ge). Slightly high C-V stretch-out was observed with 40% Ge, due to interface charge density. Gate leakage current densities (J_g) of $HfSiO_2$ dielectrics on SiGe channels were lower than SiO_2 on Si channel devices by more than 3×10^2 times and comparable with optimized $HfSiO_2$ dielectrics on Si channels [3] (Fig. 3). Low threshold voltages (V_{th}) of -0.41 V (25% Ge) and -0.24 V (40% Ge) were obtained from 1 μm gate SiGe pMOSFETs, which are significantly lower than -0.81 V of Si pMOSFETs with identical gate dielectric and metal gate (Fig. 4). Lower V_{th} with increasing higher Ge% is attributed to smaller band gap energy of SiGe (or larger valence band offset relative to Si), which requires smaller band bending (or surface potential) for channel inversion. This behavior is in good agreement with positive V_{th} reported on other Ge pMOSFETs [4–5]. Large V_{th} roll-off observed in 40% Ge might be due to insufficient halo doping activation. N-type dopant implantation into SiGe or Ge suffers from low solid solubility and activation efficiency. Fig. 5 compares I_d-V_g of SiGe and Si channel pMOSFETs. Subthreshold swing (SS) of SiGe channels (70–78 mV/dec) are comparable with reference Si channel devices. Gate induced drain leakage (GIDL) current, however, increases when Ge concentration increases, which is attributed to high band-to-band tunneling (BTBT) of small band gap channel materials [6] and high interface trap density. Fig. 6 shows that GIDL currents are governed either by gate leakage current (25% Ge) or substrate current (40% Ge), which confirms a high BTBT current on small band gap energy channels. Note that GIDL and SS characteristics are improved by reducing epi-SiGe channel thicknesses deposited on Si substrates (Fig. 7), because relatively small epi-SiGe portion is included in electrostatic field. Smaller band gap energy (E_g,) and higher permittivity (ε) of SiGe than those of Si tend to degrade off-state characteristics in SiGe-on-Si heterostructures. Well-behaved, short channel I_d-V_g of SiGe pMOSFETs (25% and 40% Ge) are shown in Fig. 8. Simulated (Fig. 9) and measured (Fig. 10) C-V curves with varying Ge concentration provide further device characteristics. If non-ideal effects are not taken into account in simulation, two parameters (ϕ_{ms} and Q_i) should have little difference with Ge%. The V_{fb} is a function of metal-semiconductor workfunction (ϕ_{ms}) and interface charge density (Q_i). Therefore, the simulation shows almost identical flat band voltage (V_{fb}) with increasing Ge%. However, V_{th} is a function of depletion charges (Q_d) and surface potential (ϕ_s), which strongly depend on E_g (or n_i) and ε of SiGe with varying Ge%. As a result, V_{th} decreases when Ge% increases. Measured C-V curves exhibited slightly high V_{fb} and stretch-out behavior due presumably to high Q_i of high Ge%. V_{th} showed an expected trend. Fig. 11 compares improved normalized transconductance (G_m) of SiGe channels over universal SiO_2/Si channel and optimized high-k dielectric/metal gate Si channel. A mobility enhancement of 50% and 13% from 40% and 25% SiGe pMOSFETs, respectively, over universal mobility have been readily achieved in Fig. 12.

Conclusions

We have demonstrated high-mobility pMOSFETs on high-quality epitaxial SiGe films selectively grown on Si substrates using a CVD system. The gate stack of $HfSiO_2$ on SiGe channel exhibited minimal C-V hysteresis (≤ 20 mV) and low gate leakage current (~3×10^2 times lower than SiO_2/Si channel) at EOT of 14 Å. V_{th}, V_{th} roll-off, SS, and GIDL become lower when Ge% increases in the SiGe channel. This is attributed to varying E_g (or n_i) and ε of SiGe. We have achieved high on-state current (or mobility), while effectively suppressing off-state characteristics comparable to an optimized Si channel or Si/SiGe quantum well pMOSFETs.

References

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[3] P. D. Kirsch IEDM, p. 629, 2006.
[4] P.Zimmerman et al., IEDM, p.655, 2006.
[5] O.Weber et al., IEDM, p.143, 2005.
[6] K.Saraswat et al., IEDM, p.659, 2006.

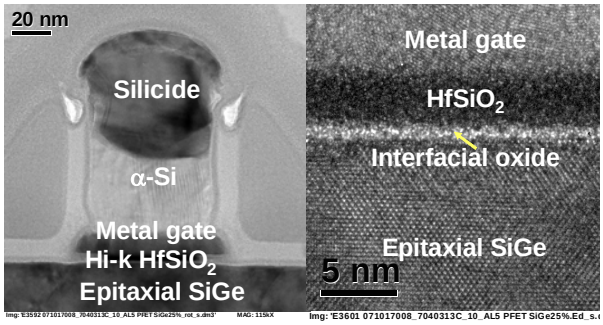

Fig.1 (a)Bright-field and (b) high-resolution XTEM images of gate stack with $HfSiO_2$ high-k gate dielectrics and metal gates fabricated on high-quality epitaxial SiGe layers selectively grown on Si (100) substrates using a CVD system.

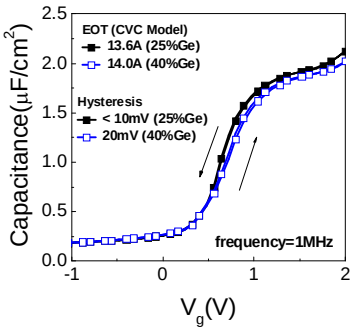

Fig.2 C-V of SiGe MOS capacitors with low EOT and minimal hysteresis. (40Å $HfSiO_2$). Slightly higher C-V stretch-out observed with 40% Ge due to higher interface charge density.

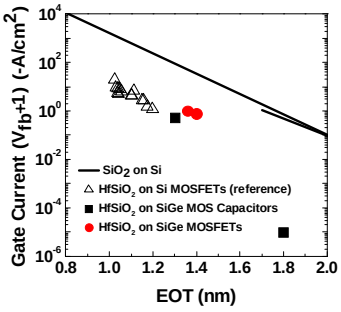

Fig.3 Gate leakage current density (J_g) of $HfSiO_2$ dielectric on SiGe channel pMOSFETs. (~$3x10^2$ lower than SiO_2/Si channel) at EOT of 14Å.

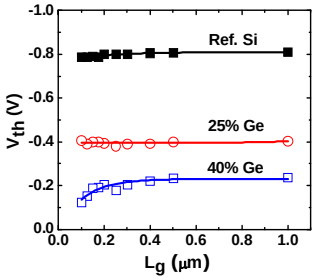

Fig.4 Low V_t of -0.41V (25% Ge) and -0.24V (40% Ge) of SiGe channel pMOSFETs, which are significantly lower than V_t of ref. Si channel.

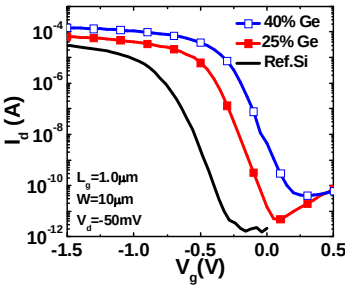

Fig.5 SS(70~78mV/dec) of SiGe channels comparable with ref. Si channel. GIDL, however, increases due to BTBT current when Ge % increases.

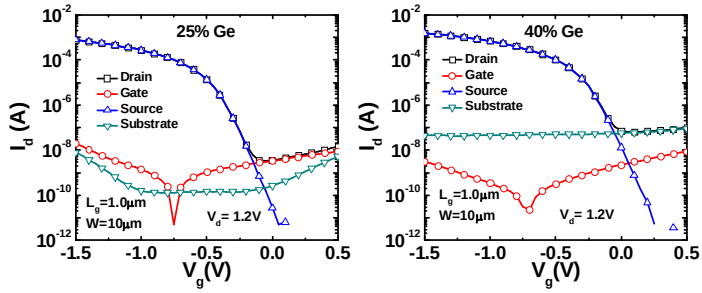

Fig.6 GIDL currents are governed either by gate leakage current (25% Ge) or substrate current (40% Ge), which confirms a high BTBT current on small band gap energy channel materials (or high Ge %).

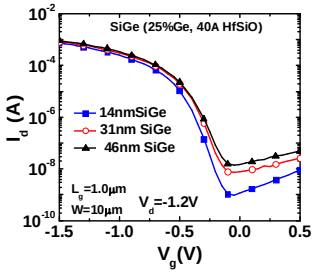

Fig.7 Improved GIDL and SS characteristics by reducing SiGe channel thicknesses due to relatively small SiGe portion in electrostatic field.

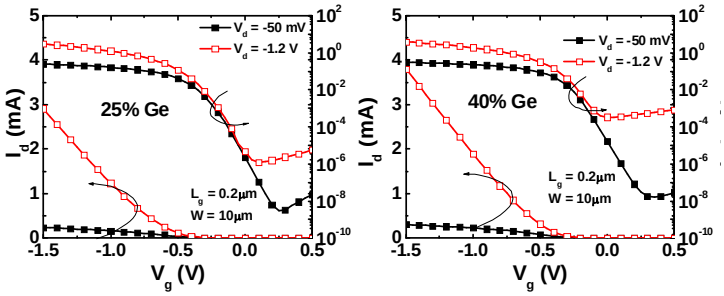

Fig.8 Well behaved short channel I_d-V_g of SiGe channel pMOSFETs (25% and 40% Ge).

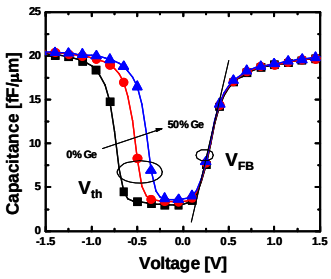

Fig.9 Simulated C-V shows identical V_{fb} and varying V_{th} with increasing Ge% due to changes in depletion charge and surface potential.

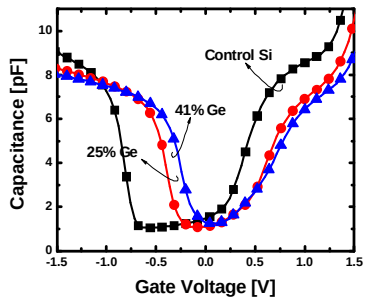

Fig.10 Measured C-V exhibit slightly high V_{fb} and stretch-out for high Ge% due to higher Q_i. V_{th} shows an expected trend as simulation results.

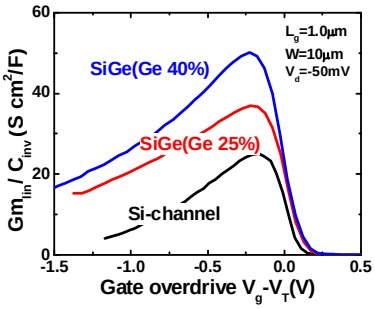

Fig.11 Normalized G_m of SiGe channels over universal SiO_2/Si channel and optimized high-k dielectric/metal gate Si channel.

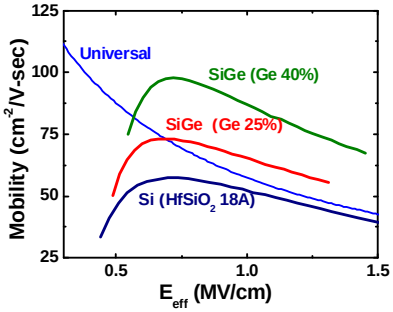

Fig.12 A mobility enhancement of 50% and 13% from 40% and 25% SiGe channel pMOSFETs, respectively, over universal mobility.