

MITIGATION OF CMOS VARIABILITY WITH METAL GATE

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ABSTRACT

Variability due to Fermi level pinning at polysilicon gate grain boundary is examined as an additional source of intrinsic parameter fluctuation. V_t variation with metal gate to avoid the variation is found to be mitigated with the measurement of nMOSFETs with an identical process except gate stack. The statistical variation of intrinsic gate delay and static noise margin of the 6T SRAM cell is predicted for future technology nodes using Monte Carlo circuit simulation with a process/physics-based compact model. It is found that the variability can be suppressed by ~35% with adopting metal gate for 32 nm technology node.

INTRODUCTION

The 'local' variability due to intrinsic parameter fluctuation will be a major challenge to scale down CMOS devices. The variation in number and position of dopant atoms in the channel region has been identified as the most important source of the intrinsic parameter fluctuation. Recently, the Fermi level pinning at polysilicon gate grain boundary has been suggested as an additional source of intrinsic parameter fluctuation [1]. In this paper, we examine the variability of polysilicon gate compared to metal gate process for the first time with an experiment. The performance and yield of CMOS circuits for future technology nodes is also predicted from the mitigation of variability with metal gate using process/physics-based compact model-UFPDB/SPICE3 [2].

MITIGATION OF V_t VARIATION WITH METAL-GATE

The fabrication flow of these two devices is identical, except for the gate stack process to identify the variability of polysilicon grain boundary. The 2.0 nm Hf-based dielectric/band-edge n-type metal gate stack was used for metal gated nMOSFET fabrication. For the comparison, the conventional n+ polysilicon nMOSFET was fabricated using 2.0 nm of SiO₂. The polysilicon grain boundary, which yields the additional variability due to Fermi level pinning, is shown in the AFM image of Fig. 1. About 800 devices were measured for each device dimension. Note that narrow width devices with polysilicon gate show higher V_t variation, while the devices with metal gate do not. The results are consistent with the simulation study [1], which shows higher V_t change when the grain boundary is located along gate width direction. Narrow width device is more vulnerable to variation because higher portion of the grain boundary is located along the gate width direction in the device.

PROCESS/PHYSICS-BASED COMPACT MODEL

There have been several studies using TCAD [3] and empirical compact models. However, a limit to the device level and unreliable parameter correlation in the model card are an inherent disadvantage for the methods, respectively. UFPDB/SPICE3, which is a process/physics-based compact model, is used to predict the performance and yield of CMOS circuits for future technology nodes. Fig. 3 and 4 show the model calibration of gate and drain characteristics, respectively, for 32 nm nMOSFET with high-k/metal gate. There was reasonable process parameter tuning in the model card, such as channel doping (Nbl), EOT (toxf), retrograde channel depth (tb), etc. and no empirical parameter tuning for the calibration.

Fig. 5 shows good agreement of the SPICE model with measurement data for saturation V_t and drive current versus channel length. To match the model with the measurement data, only one model parameter (i.e., halo doping density (Nhalo)) was tuned. Thus, the problem of the parameter correlation in the model card can be avoided with UFPDB for Monte Carlo (MC) circuit simulation.

MONTE CARLO CIRCUIT SIMULATION

To predict the performance and yield of CMOS circuits for future technology nodes, the model parameters in the UFPDB model card were set to meet the device parameter in the 2007 ITRS [4] for each technology node. We assumed that the random dopant effect is dominant and other intrinsic fluctuations were ignored. Channel doping density (Nbl) and gate workfunction (Wkf) in the model card were chosen to represent the random dopants and polysilicon grain effects, respectively. σ_{Nbl} and σ_{Wkf} were tuned to match σ_{V_t} with the results from 3D TCAD [5] for each channel length through MC simulation. Fig. 6 shows the simulation results of V_t variation, taking into account the intrinsic fluctuation for $L_g = 32$ nm nMOSFETs. The statistical data is derived from the 10,000X MC simulation. Fig. 7 shows the average intrinsic gate delay ($\langle\text{delay}\rangle$) and its standard deviation (σ_{delay}) for each channel length from MC circuit simulation with a 5 stage ring oscillator. The σ_{delay} increases abruptly at $L_g = 13$ nm, while $\langle\text{delay}\rangle$ reduces. As a results, the normalized delay variation is up to 10% at $L_g = 13$ nm for polysilicon gate, which can be suppressed by ~35% when adopting metal gate as shown in Fig. 8. We also performed MC simulations of the static noise margin (SNM) of typical 6T SRAM cells as shown in Fig. 9. In Fig. 10, the average SNM ($\langle\text{SNM}\rangle$) reduces down to less than 100 mV at $L_g = 13$ nm. The standard deviation of SNM (σ_{SNM}) increases rapidly as channel length scales down because σ_{V_t} increases and V_{dd} decreases. A higher rate of zero SNM in poly gate as shown in Fig. 11 yields lower $\langle\text{SNM}\rangle$ in Fig. 10. The normalized SNM variation is up to 60% at $L_g = 13$ nm for polysilicon gate. This unacceptable variation is reduced by ~35% when adopting metal gate as shown in Fig. 12.

CONCLUSION

The mitigation of V_t variation with metal gate was examined by experiment. The statistical variation of delay and SNM for the 32 nm technology node is predicted using MC circuit simulation with process/physics-based compact model. It is found that the variability is unacceptable and can be suppressed by ~35% when adopting metal gate for the 32 nm technology node.

ACKNOWLEDGMENTS

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REFERENCES

- [1] A. R. Brown et al., Proc. ESSDERC 2006, 451 (2006)
- [2] UFSOI MOSFET Model ver. 7.5, Univ. of Florida (www.soi.tec.ufl.edu)
- [3] A. Asenov et al., IEEE T-ED, pp. 1837, Sep. 2003.
- [4] International Technology Roadmap for Semiconductors. Austin, TX: SIA/SEMATECH, 2007.
- [5] A. Asenov, VLSI Tech. 2007, 86, 2007

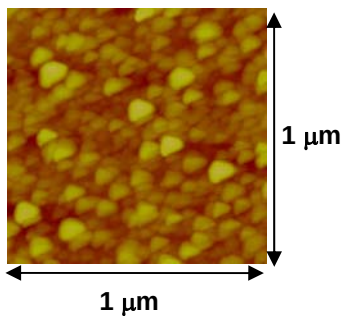


FIGURE 1 AFM IMAGE OF POLYSILICON GRAINS

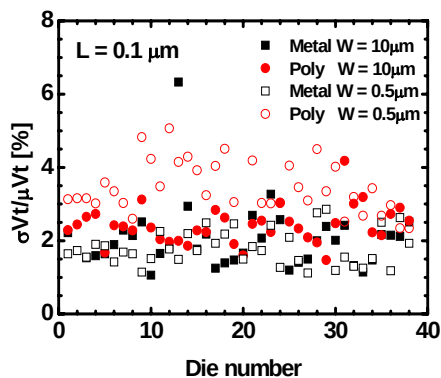


FIGURE 2. COMPARISON OF VT VARIATION BETWEEN METAL AND POLY GATE DEVICES.

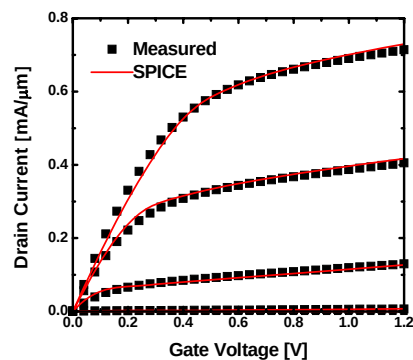


FIGURE 3. MODEL CALIBRATION OF DRAIN CHARACTERISTICS FOR NMOSFET WITH $L_G=32\text{nm}$

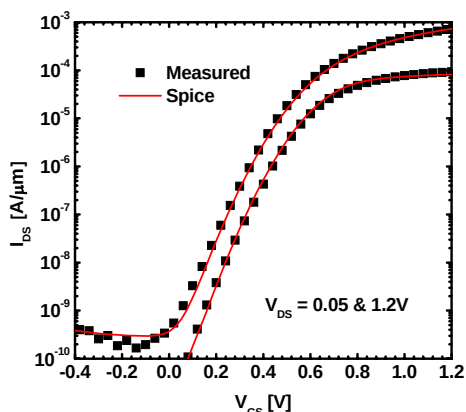


FIGURE 4 MODEL CALIBRATION OF GATE CHARACTERISTICS FOR NMOSFET WITH $L_G=32\text{nm}$

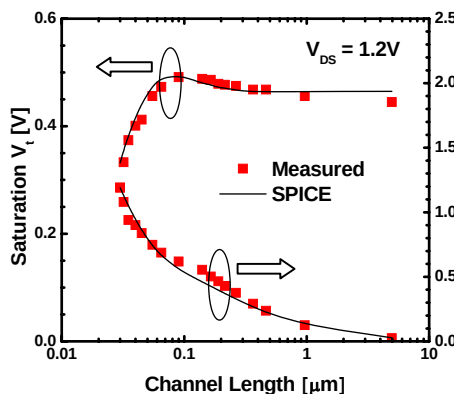


FIGURE 5. MODEL CALIBRATION OF SATURATION V_T AND DRAIN CURRENT CHARACTERISTICS FOR NMOSFET

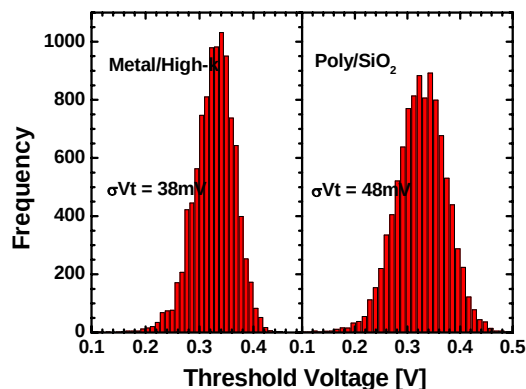


FIGURE 6. VT VARIATION RESULTS FROM MC SIMULATION TAKING INTO ACCOUNT RANDOM DOPING AND POLY GRAIN FOR NMOSFET WITH $L_G=32\text{nm}$

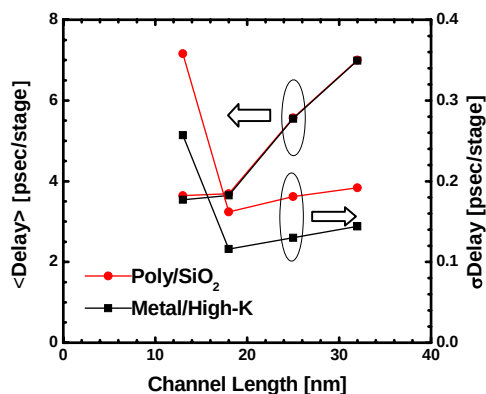


FIGURE 7. SIMULATED THE AVERAGE AND STANDARD DEVIATION OF INTRINSIC GATE DELAY USING MONTE CARLO UFPDB: 5 STGES RING OSCILLATOR, UNLOADED INVERTER, $FO=1$.

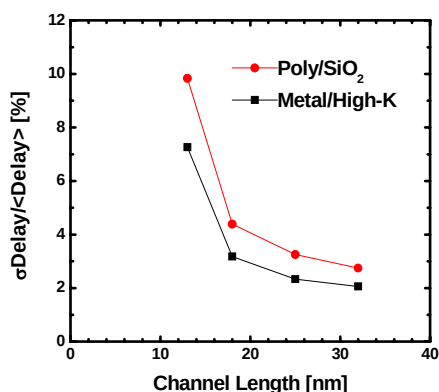


FIGURE 8 NORMALIZED STANDARD DEVIATION OF INTRINSIC GATE DELAY

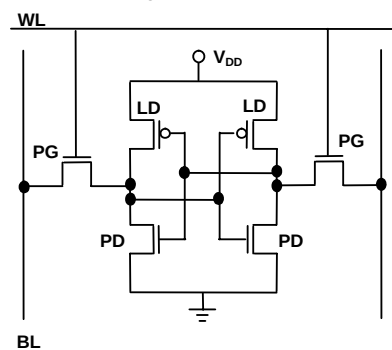


FIGURE 9 CIRCUIT SCHEMATICS OF 6T SRAM: PD (PULL DOWN), PG (PASS GATE), LD (LOAD), $W_{PG}:W_{PD} = 1:2$.

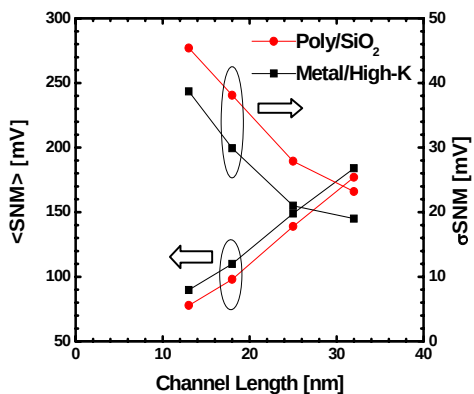


FIGURE 10 SIMULATED THE AVERAGE AND STANDARD DEVIATION OF STATIC NOISE MARGIN OF 6T SRAM CELL USING MONTE CARLO UFPDB.

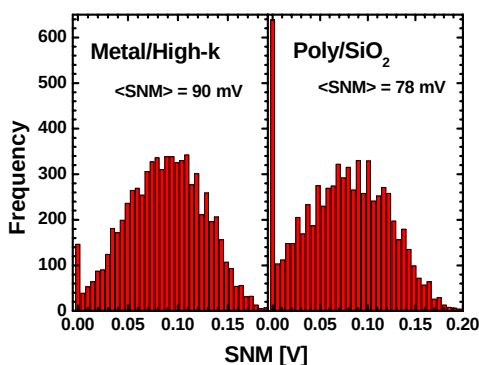


FIGURE 11. SNM VARIATION RESULTS FROM MC SIMULATION TAKING INTO ACCOUNT RANDOM DOPING AND POLY GRAIN FOR NMOSFET WITH $L_G=13\text{nm}$

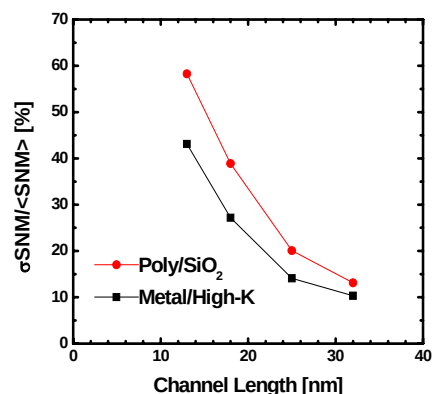


FIGURE 12 NORMALIZED STANDARD DEVIATION OF STATIC NOISE MARGIN