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Simulation of Material and Strain Engineering of Tunneling Field-Effect Transistor with Subthreshold Swing below 60 mV/decade

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ABSTRACT

The tunneling field-effect transistor (TFET) is studied as an alternative device to conventional MOSFET using 2-dimensional (2-D) device simulation. Strain and material engineering are employed to further boost the band-to-band tunneling rate in TFET by utilizing a smaller bandgap. This gives rise to a steeper subthreshold swing S and higher on-state current I_{on}. Low power supply voltage V_{DD} coupled with bandgap engineering helps to enable further scaling of transistor size.

1. INTRODUCTION

TFET [1]-[3] has been proposed as an alternative device to alleviate the power consumption issue faced by CMOS device scaling. Such a gated p-i-n diode exploits gate-controlled band-to-band tunneling (BTBT) between the source and the channel to realize steep subthreshold swing of sub-60 mV/decade. However, one major drawback of the proposed Si TFET is that its on-state current I_{on} is significantly lower than that of CMOS transistors and below the requirement set in the International Roadmap for Semiconductor (ITRS). In this paper, the TFET device is optimized for higher performance through strain and material engineering. The lower bandgap material enhances BTBT rate that boost I_{on} and enables power supply voltage V_{DD} scaling for low power consumption.

2. DEVICE STRUCTURE AND CONCEPT

The TFET device structure considered is as shown in Fig. 1(a). A semiconductor layer consisting of Si, strained Si, Ge or InAs on a silicon-dioxide (SiO_2) or buried oxide serves as the device layer. The gate stack comprises of a metal electrode with a gate work function of 4.05 eV, and a HfO_2 high-k gate dielectric of 5 nm physical thickness with a relative dielectric permittivity of 25. The peak of drain and source Gaussian doping are assumed, respectively, to be 10^{18} cm^{-3} and 10^{20} cm^{-3} with a gradient ~3nm/dec. The channel is p-type doped with a concentration of 5×10^{16} cm^{-3}. Fig. 1(b) shows another TFET structure that employs a hetero-source with a narrower bandgap material for higher BTBT rate. Synopsys Technology Computer-Aided Design (TCAD) tools were used. The BTBT rate is modeled using Kane's model [4]

$$G_{BTBT} = A\frac{\xi^2}{E_g^{1/2}}.\exp\left(-B\frac{E_g^{3/2}}{\xi}\right) \quad (1)$$

where E_g is the energy bandgap of the material through which tunneling occurs, and ξ is the magnitude of the electric field. A and B are function of effective masses of the material. A study of the BTBT rate for different materials is depicted in Fig. 2. In order to overcome the low I_{on} of Si TFET, higher BTBT rate is required. This could be achieved by employing strained Si (biaxial tensile stress ~1.5 GPa), or narrower bandgap material like Ge, InAs, and InSb. The BTBT rate increases at lower electric field, with increasing abrupt electric field dependence.

3. RESULTS AND DISCUSSION

A. Strain Engineering

Strain has been employed in conventional CMOS transistor to boost their performance. Similarly, strain engineering could also be employed to TFET. One way to achieve this is to use strained Si-on-insulator (SSOI) wafers. Fig. 3 illustrates the impact of various types of stresses of 1.5 GPa on TFET's performance. The application of strain/stress to a material can change the bandgap of the material. As such, it is the narrower bandgap that gives rise to the higher BTBT rate. This increases the I_{on} by 3-6 times and improves the average subthreshold swing S_{ave} from 65 mV/dec. to 55 mV/dec. In addition, the threshold voltage V_T is also reduced. Due to the narrower bandgap, I_{off} has also increased. Fig. 4 depicts the summary of I_{on} as a function of stress for biaxial and uniaxial tensile stress as the former is most effective. The stress-induced bandgap narrowing (BGN) effect is more pronounced with biaxial tensile stress than with uniaxial tensile stress, giving rise to higher I_{on} enhancement.

B. Hetero-structure Engineering

One way to optimize the TFET structure is to adopt a hetero-source structure as shown in Fig. 1(b). The larger bandgap in the channel and drain regions reduces tunneling near the drain, while a narrower bandgap material at the source enhances the BTBT rate. To study this concept, a Si TFET with SiGe hetero-source is considered. By incorporating Ge into the source region to form SiGe, the bandgap E_g reduces, and this narrows the tunneling width ω_T between the Si channel and the SiGe source. Fig. 5 illustrates the energy band diagram of Si TFET devices with Si and $Si_{0.6}Ge_{0.4}$ source, respectively. With narrower ω_T, electrons are able to tunnel more easily from the $Si_{0.6}Ge_{0.4}$ source to the Si channel. As such, higher I_{on} is achieved with reduced V_T and steeper S_{ave} (Fig. 6). At a Ge content of 40%, S_{ave} improves from 65 mV/dec. to 35 mV/dec, with I_{on} increasing by more than an order of magnitude. It is observed that I_{on} increases exponentially with increasing Ge concentration in the source region (Fig. 7).

C. Material Engineering

In order to scale V_{DD} with device scaling, new materials are needed for TFET as I_{on} remains low for Si TFET at lower V_{DD}. The gate transfer characteristics for Si, Ge and InAs TFETs are shown in Fig. 8. In general, use of lower bandgap material enables TFET to operate at a lower V_{DD} with reduced V_T, improved S_{ave}, and higher I_{on}. However, one drawback of narrow bandgap material is the increased I_{off}. The V_{DD} scaling scenario is illustrated in Fig. 9. It is obvious that Si is definitely not the material of choice for TFET. Ge TFET has the potential to operate at low V_{DD} with sufficient I_{on}. For ultra-low voltage operation, InAs with E_g of 0.36 eV is needed. With present projection of T_{ox} scaling, both Ge and InAs TFETs have the potential to scale beyond conventional CMOS roadmap.

5. CONCLUSION

The TFET technology is studied through 2-D device simulation. Strain and material engineering is employed to boost the performance of TFET. The incorporation of narrower bandgap material helps to increase the BTBT rate, and achieve steeper S and higher I_{on} at lower V_{DD}. Thus, low V_{DD} coupled with bandgap engineering helps to pave the way for transistor downscaling while maintaining low power consumption.

REFERENCES

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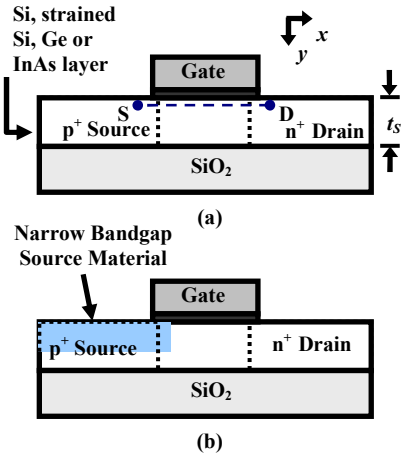

Fig. 1. Schematic of (a) TFET with various types of channel layer, and (b) TFET with source hetero-junction. For an n-channel TFET, the drain is doped n^+ while the source is doped p^+.

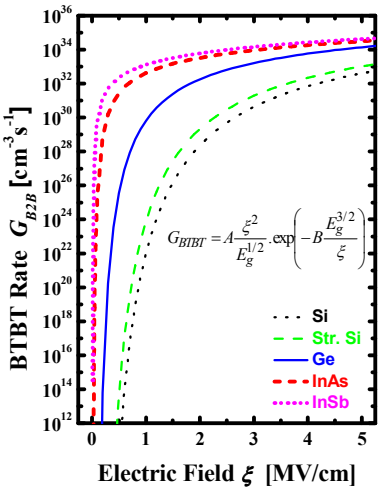

Fig. 2. Study of band-to-band tunneling rate as a function of electric field for various semiconductor materials. In general, lower bandgap materials like Ge or InAs achieves higher BTBT rate.

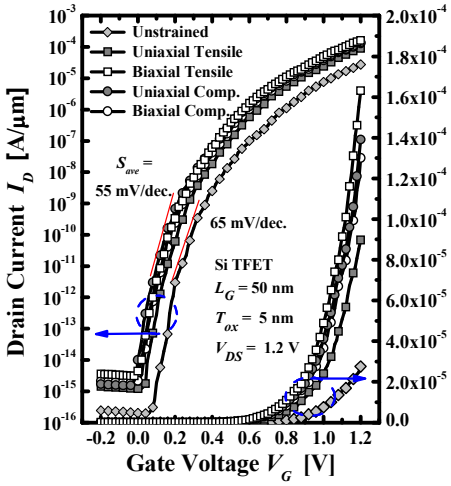

Fig. 3. (a) Simulated gate transfer characteristics for unstrained and strained Si TFET under various type of stress. The stress applied here is 1.5 GPa. Biaxial tensile stress is more effective in boosting I_{on}.

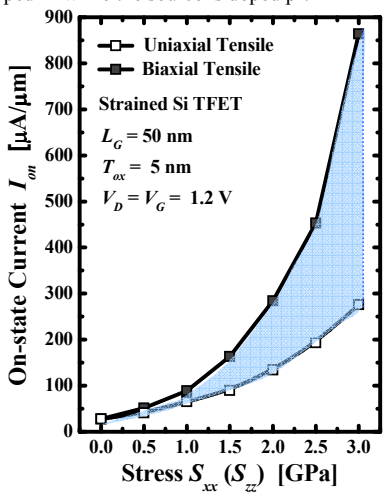

Fig. 4. On-state current I_{on} as a function of stress for uniaxial stress and biaxial stress Si TFET. The shaded region enclosed the I_{on} achievable by applying different types of stresses.

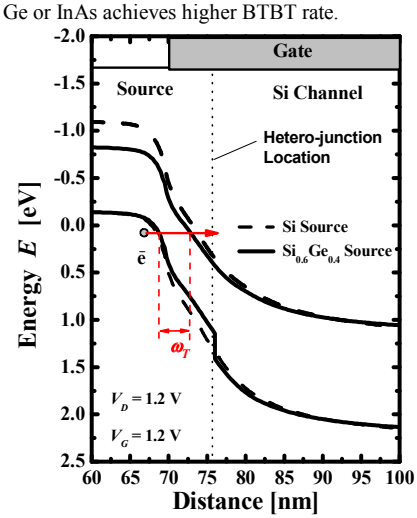

Fig. 5. Extracted energy band diagrams along the source to channel direction near the surface. In the on-state, tunneling occurs at the source-side. Narrower bandgap SiGe results in a smaller ω_T.

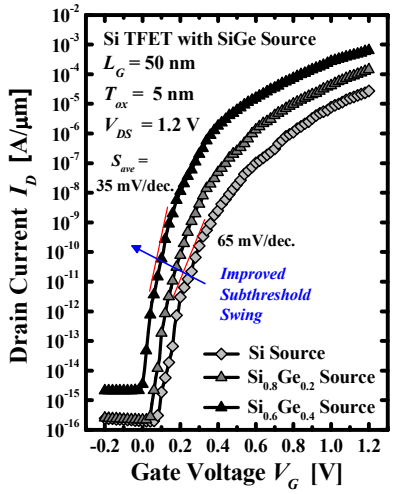

Fig. 6. Plot of I_D-V_G as a function of Ge content in the source. Lower V_T, higher I_{on} and improved S are achievable with increasing Ge concentration in the source region.

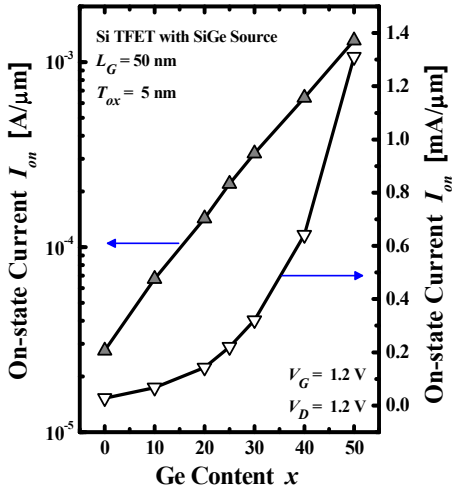

Fig. 7. On-state current I_{on} increases exponentially with increasing Ge concentration in the source region. This is a direct result of the narrower tunneling width with SiGe hetero-junction source.

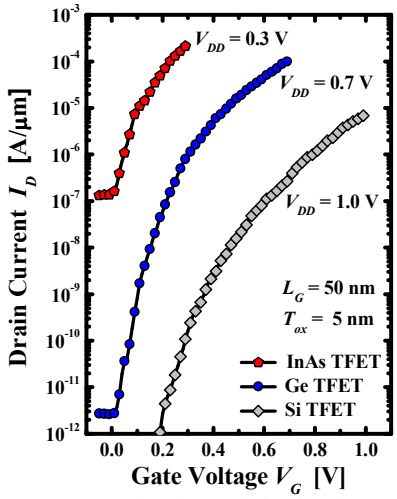

Fig. 8. Gate transfer characteristics for Si, Ge, and InAs TFETs. Narrower bandgap materials result in a significantly higher I_{on}. However, the I_{off} is also significantly higher.

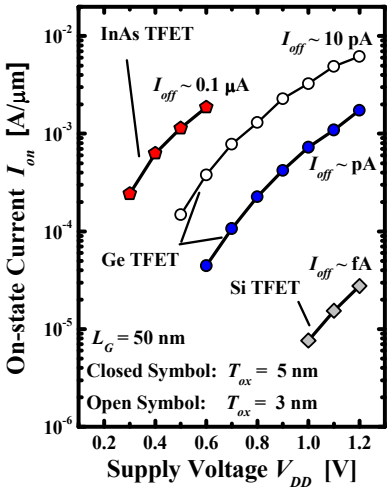

Fig. 9. V_{DD} scaling scenario for Si, Ge, and InAs TFETs. Narrower bandgap materials are required to maintain sufficient I_{on} as V_{DD} scales down.