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Understanding the effect of laser anneal on LSTP 45nm node MOS transistor electrical parameters

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Abstract

The 45nm technological node MOS transistor has been optimized thanks to DSA (dynamic surface annealing) technique, and an in-depth analysis of the MOS transistors electrical parameters is provided for the first time. This anneal, immediately following the main dopants activation spike anneal, is shown to improve both Cox and access resistance thanks to the dopants over-activation. However, at too high laser power, it reduces the carriers mobility and the hot carriers related lifetime because of interface states generation. Thus, a compromise has to be found for the saturation current optimization.

Introduction

In order to meet the 45nm node requirements, making thin and unresistive junctions is one of the key challenges, at least with bulk silicon technologies where the junction thickness is determined by the dopants implant and diffusion. The control of the junction thickness directly impacts the short channel effects, while the source and drain activation impacts the saturation current, via the access resistance. Using a laser anneal immediately after the main dopants activation spike anneal was shown to increase the dopant activation by enhancing the solubility limit, without any diffusion process [1-4]. Furthermore, over-activating the gate dopants also allows increasing the oxide capacitance by reducing the polydepletion.

However, the impact of the laser anneal on the second order parameters such as device mobility, access resistance and interface quality still has to be quantified and understood in order to allow the optimization of the laser conditions.

Experimental conditions: process parameters

The following experiments were led on our 45nm node technology platform [5] on the LSTP (low stand-by power) device, featuring traditional SiON gate dielectric with polysilicon gate, <100> rotated substrate for the PMOS mobility optimization, and CESL (contact etch stop layer) stress / SMT (stress memory technique) combination for the NMOS optimization via tensile stress [6].

By changing the laser power, various silicon surface anneal temperatures where explored, between 1030°C and 1320°C, plus a no laser anneal reference (17 wafers tested).

Experimental conditions: measurement methodology

The effect of the laser anneal on lateral junctions diffusion could be measured directly on the transistors thanks to a capacitance-based methodology [7] allowing a precise (<1nm) direct measurement of the effective channel length. Our method is based on the proportionality of the gate-to-channel capacitance to the electric length, with adequate parasitic capacitances measurement (fig. 1). The poly length was measured in the same way on transistors without SDE (Source and Drain Extensions) and pocket implants, and therefore the total overlap length could be computed.

The low field mobility was computed using the transconductance gain (β) of the transistor measured with the Hamer method [8]. Whereas it only monitors the mobility at low field, as an extrapolation at zero inversion charge, it is actually representative of our LSTP technology where the working point is at relatively low transverse field, due to a low Vdd and a high threshold voltage. Furthermore, it is applicable to the short gate length transistors, providing the electric gate length is known, thanks to an intrinsic substraction of the parasitic resistances effect. The effective mobility was also measured on the long transistors by the conventional split CV method [9].

The access resistances were computed from the Hamer method parameters θ and β [10]. This method allows the determination of the series resistance without any assumption neither on the mobility nor on the gate length. Qualitative indications on the interface states density have been obtained from the maximum charge pumping current, even if, due to thin oxide related gate leakage, effective traps density computation is problematic. Finally, the saturation current at a constant gate voltage overdrive (Vg-Vth) was measured, in order to get a global performance indicator while getting rid of the threshold voltage variations.

Impact of the laser on the electrical parameters

First, the laser annealing is shown to have very limited effect on the lateral dopants diffusion. Indeed, on the N channel transistor, the maximum overlap length variation is around 1nm, close to the technique precision and the process dispersion (fig. 2).

If we examine the effect of the laser annealing on the Ion performance measured at constant gate voltage overdrive, we show completely different behaviours of the NMOS and PMOS. NMOS saturation current is improved by 6% in the no laser to 1200°C laser anneal range, then slightly degraded at higher temperature (fig. 3). In the meanwhile, the PMOS transistor exhibits very low effect under 1200°C, but significant improvement at high laser temperature. However, the HCI (hot carriers injection) related degradation increases when the temperature is increased above 1200°C (fig. 4) ; thus, a compromise has to be found between, NMOS and PMOS performance and reliability.

This different behaviour between NMOS and PMOS can be explained by the measurement of the Cox and access resistance. Indeed, whereas the PMOS Cox increases continuously over all the temperature range (fig. 5), the NMOS Cox saturates over 1200°C, explaining the Ion current optimum. The strong improvement of the PMOS access resistance (fig. 6) at high temperature also explains the Ion improvement in this range, whereas the NMOS access resistance improvement is spread over the temperature range (fig.7).

However, the improvement of the Cox and Rsd should theoretically induce a stronger Ion increase, especially for the PMOS in the low temperature range. But if we examine the low field mobility (μ_0) as a function of the laser temperature (fig. 8), we notice degradation at high laser temperature, in particular above 1200°C. This transport degradation can also be shown on long channel transistors (L=10µm) thanks to split-CV measurements (fig. 9), but cannot be explained by a channel dopants activation. Indeed, if we compute the channel doping by integrating the measured depletion charge, no effective doping difference can be detected (fig. 10).

Considering also that the mobility degradation is more pronounced at low transverse field than at high field (but still very effective on the performance, due to a low field working point), it seems to be linked to Coulomb scattering, and possibly to interface traps density. This can be evidenced by the charge pumping current, increased when increasing the laser temperature, both on the nominal and high gate length transistor (fig. 11), explaining both the mobility and the HCI lifetime evolution, as HCI degradation is induced by interface states generation.

Conclusion

The NMOS and PMOS transistors saturation currents can be improved by the additional laser anneal, thanks to Cox and Rsd improvement. However, for the PMOS transistor, the improvement is mainly seen over 1200°C anneal temperature; in this temperature range, the mobility and HCI lifetime are degraded, for NMOS and PMOS, due to interface states generation. Thus, a trade-off has to be found between NMOS and PMOS performance optimization and lifetime. These results will have to be taken into account for multiple laser anneal processes under study for the next technological node [11-12].

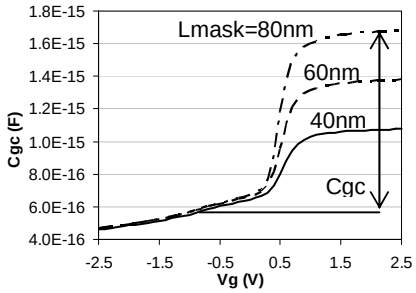

Figure 1

Gate to channel capactitance for several gate lengths. After substraction of the parasitics, the Cgc is proportional to the channel length, and allows to extract Leff. The curves are measured on arrays of transistors.

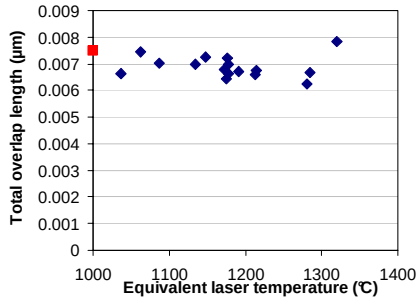

Figure 2

Total overlap length on the n channel transistor (Lmask=40nm), source and drain sides. Diamonds represent the mean value for transistors with laser anneal. Square is the reference wafer.

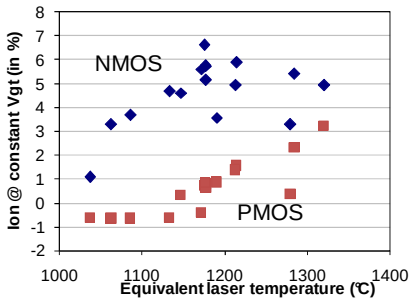

Figure 3

Saturation current measured at constant gate voltage overdrive (Vg-Vth). Relative variation as a function of the laser anneal temperature, in comparison with the reference with no laser anneal. Diamonds: NMOS. Squares: PMOS, Lmask=40nm

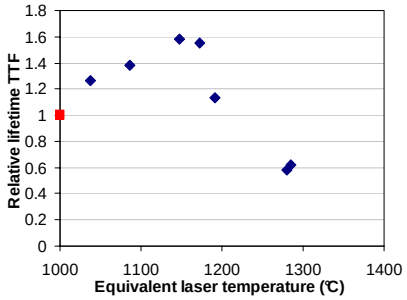

Figure 4

Hot carriers degradation related relative lifetime (NMOS, Lmask=40nm), normalized at constant saturation current, and in comparison with the no laser anneal reference wafer

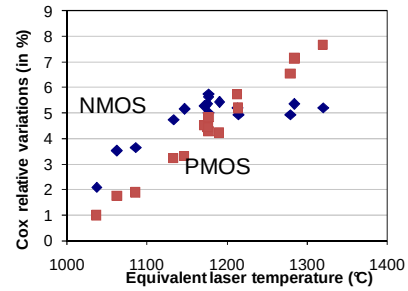

Figure 5

Oxide capacitance measured in inversion regime, at the nominal technology Vdd (1.1V). Relative variation as a function of the laser anneal temperature, in comparison with the reference with no laser anneal. Diamonds: NMOS. Squares: PMOS.

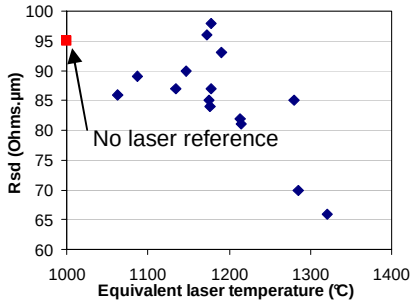

Figure 6

Total normalized access resistance on the NMOS transistor. Diamonds represent the mean value for transistors with laser anneal. Square is the reference wafer.

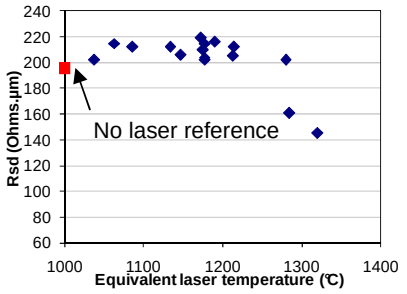

Figure 7

Total normalized access resistance on the PMOS transistor. Diamonds represent the mean value for transistors with laser anneal. Square is the reference wafer.

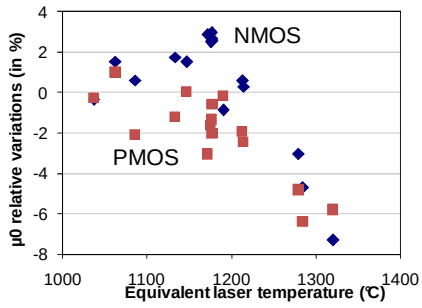

Figure 8

Low field mobility (μ_0) computed from the transconductance gain, effective length and oxide capacitance. Relative variation as a function of the laser anneal temperature, in comparison with the reference with no laser anneal (Lmask=40nm).

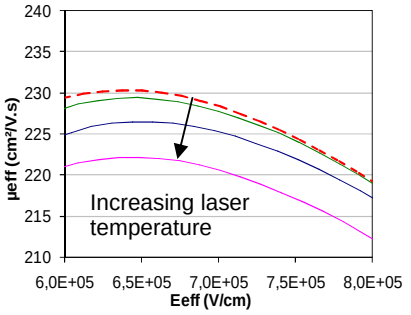

Figure 9

Effective mobility measured on W/L = 10/10µm NMOS transistor by split-CV method. Dashed line: no laser reference. Plain lines: laser anneal temperatures 1063°C, 1177°C and 1320°C

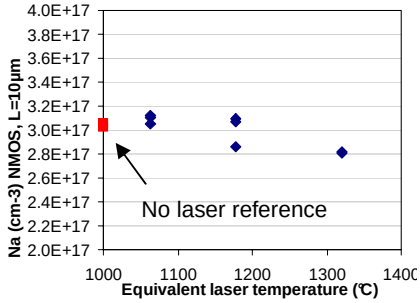

Figure 10

Effective doping measured by depletion charge integration on the gate-to-substrate capacitance, on W/L = 10/10µm NMOS.

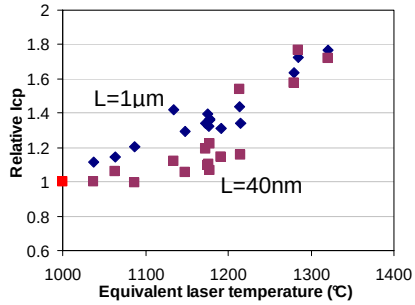

Figure 11

Max charge pumping current, in comparison with the wafer with no laser anneal, on NMOS transistor L=1µm (diamonds) and L=40nm (squares).

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