Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 876-877

B-9-1

A Study on Very High Performance Novel Balanced FD-SOI CMOSFETs on Si(110) Using Accumulation Mode Device Structure for RF Analog Circuits

Weitao Cheng[1], Akinobu Teramoto[1], ChingFoa Tye[2], Rihito Kuroda[2], Shigetoshi Sugawa[2] and Tadahiro Ohmi[1, 3]

[1] New Industry Creation Hatchery Center, [2] Graduate School of Engineering, [3]WPI Research Center, Tohoku University
Aza-Aoba 6-6-10, Aramaki, Aoba-Ku, Sendai 980-8579, Japan

1. Introduction

Recently, it is very important to improve the CMOS RF analog circuits performance[1-2] because of the obvious merits such as higher gain and lower current for Low Noise Amplifier, lower power supply, smaller distortion for mixer and so on. The performance of p-MOSFETs on Si(100) is far more dissatisfied than n-MOSFETs and limits the RF CMOS analog circuits. It has been reported the performance of p-MOSFETs has been greatly improved on Si(110) surface [3,4]. However, the degradation of electron mobility and 1/f noise in n-MOSFETs on Si(110) must be solved. In this paper, a new approach has been carried out to greatly improve the CMOS performance by introducing the accumulation-mode (AM) n-MOSFET on Si(110) for the first time. In this novel balanced FD-SOI CMOS, the current drivability in both n- and p-MOSFETs is balanced and is larger than that in n-MOSFET on Si(100). This novel balanced CMOS performs ideal inverter characteristics with the same gate width for n- and p-MOSFETs and very high switching speed compared with conventional Si(100) inversion-mode (IM) CMOS. At the same time, 1/f noise is obviously suppressed in AM n-MOSFETs on Si(110) operated at both the linear and saturation region.

2. Experimental

In this study, the novel balanced CMOS combined with AM n-MOSFET and IM p-MOSFET is shown in fig. 1. It has been fabricated on Si(110) with the same doping type SOI layers and gate Poly-Si electrodes. The SOI layers doping concentrations (N_{sub}) are 10^{15}, 10^{16}, and $2x10^{17}$ cm^{-3}. The thickness of SOI layers (T_{SOI}) is 40 nm. Surface micro-roughness is suppressed by a radical oxidation process and maintained by 5-step room temperature cleaning[5]. Gate oxides are formed by radical oxidation at 400°C[6]. B^+ ions ($1.0x10^{16}$ cm^{-2}) are implanted to gate Poly-Si layer (300 nm) for AM n- and IM p-MOSFETs. As^+ and BF^{2+} ($1.5x10^{15}$ cm^{-2}) ions are implanted to Source/Drain region for n- and p-MOSFET, respectively.

3. Results and Discussions

Fig. 2 shows the I_d-V_d characteristics of n- and p-MOSFETs on Si(110) and (100) surfaces. A novel complete balanced CMOS with the gate length of 0.35μm is realized on Si(110) surface using AM n-MOSFET and IM p-MOSFET at the first time. The current drivability of IM p-MOSFET on Si(110) is about 3 times larger than that on Si(100) surface and that of AM n-MOSFET on Si(110) is about 1.2 times larger than IM n-MOSFET on Si(100). In this novel balanced CMOS on Si(110), almost the same current drivability has been realized in both n- and p-MOSFET and is larger than that in conventional IM MOSFETs on Si(100). Fig. 3 shows the drain saturation current dependence on N_{sub}. The drain current is improved in AM n-MOSFETs, however almost no improvement in AM p-MOSFETs. The mechanism is shown in fig. 4 and 5. Fig. 4 shows the effective filed (E_{eff}) dependences of effective mobilities (μeff) on Si(100), (110) surfaces[7]. It has been observed that μeff for electron and hole on Si(110) is proportional to $E^{-0.7}$, $E^{-0.04}$. Electron mobility on Si(110) decreases steeply as increasing E_{eff}. Fig. 5 shows the improvement of the drain current in AM MOSFETs agrees well with the power of E_{eff} from mobility curves and mainly resulted from the improvement of mobility for the lower E_{eff} at AM MOSFETs operated at the same gate bias. Fig. 6 shows the ideal V_{in}-V_{out} characteristics in the novel balanced CMOS inverter with AM n-MOSFET and IM p-MOSFET on Si(110) with the same gate width because of the same current drivability in n- and pMOSFET in this balanced CMOS. The occupancy area of this balanced CMOS on Si(110) is about half of that of conventional CMOS on Si(100). Fig. 7 shows the oscillation characteristics for 101 stages of inverter chains for gate width of pMOSFET/nMOSFET=1:1 on Si(110) and 3:1 on conventional Si(100). The switching speed for Si(110) is about 2 times higher than that of Si(100) even at the gate oxide for Si(110) of 6.7nm and that for Si(100) of 3nm. These characteristics indicate that the balanced CMOS can dramatically improve the performance of future CMOS RF analog circuits. Fig. 8 shows the noise power as a function of measurement frequency. 1/f noise in AM n-MOSFET on Si(110) operated at linear region is reduced about 1 digit. Fig. 9 shows 1/f noise levels in n-MOSFETs on Si(110) operated on saturation region as a function of drain current. The slope for AM n-MOSFETs is much smaller than that for IM n-MOSFETs. This indicates a suppression of current fluctuation on bias conditions in AM devices.

3. Conclusions

In this study, we have been successful in realizing the very high performance novel balanced CMOS devices on Si(110) surface using AM FD-SOI MOSFETs with very high speed oscillation performance and very low noise. This technology is very useful for realizing advanced high performance CMOS RF analog circuits.

Acknowledgements

This work was partly supported by the project under Grant-in-Aid for Specially Promoted Research (project No. 18002004) and the project under Grant-in-Aid for Young Scientists (A) (project No. 19686019), supported by Japanese Ministry of Education, Culture, Sports, Science and Technology.

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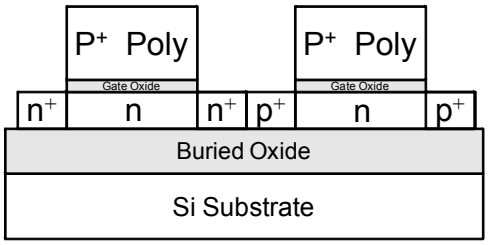

Fig. 1 Schematic of the novel balanced CMOS on Si(110) surface combined with AM n-MOSFET and IM p-MOSFET.

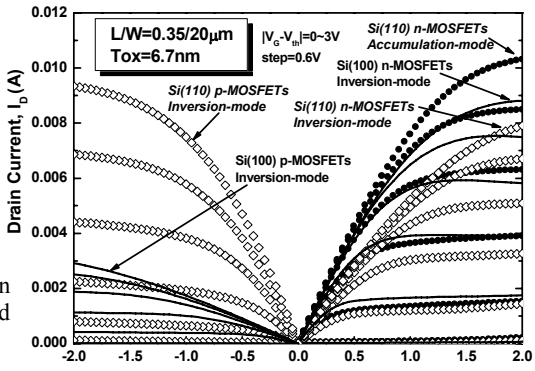

Fig. 2 I_d-V_d characteristics of n- and p-MOSFETs on Si(110) and (100) surfaces. A complete balanced CMOS is realized on Si(110) surfaces using AM n-MOSFET and IM p-MOSFET with very high current drivability. The current drivability of AM n-MOSFET on Si(110) is about 1.2 times larger than IM n-MOSFET on Si(100).

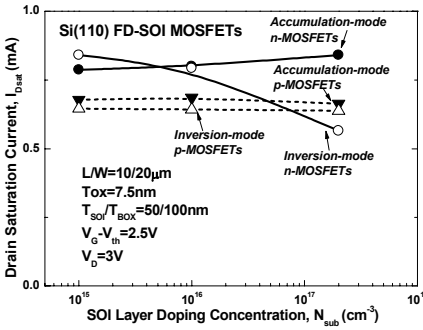

Fig. 3 Drain Saturation Current as a function of N_{sub} in n- and p-MOSFETs on Si(110). I_{Dsat} increases with increasing the N_{sub} in AM n-MOSFETs and shows no dependence on N_{sub} in p-MOSFETs.

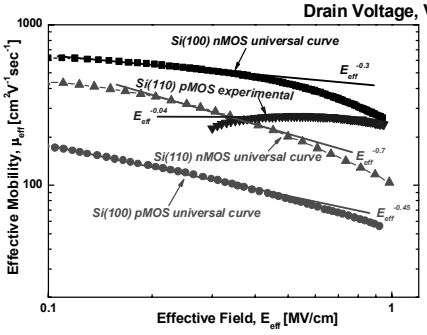

Fig. 4 E_{eff}-μ_{eff} characteristics of electrons and holes on Si(100) and (110). μ_{eff} in n-MOSFETs on Si(110) is expected to be improved most greatly by lowering E_{eff} and almost no improvement for holes on Si(110).

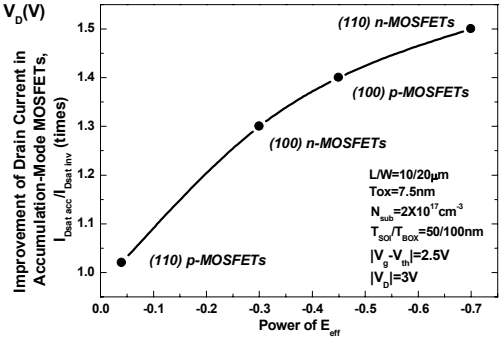

Fig. 5 I_{dsat} improvement in AM MOSFETs on Si(100) and (110) as a function of the power of E_{eff}. This result indicates the mechanism for the current improvement in AM MOSFETs is resulted from the lowering E_{eff}.

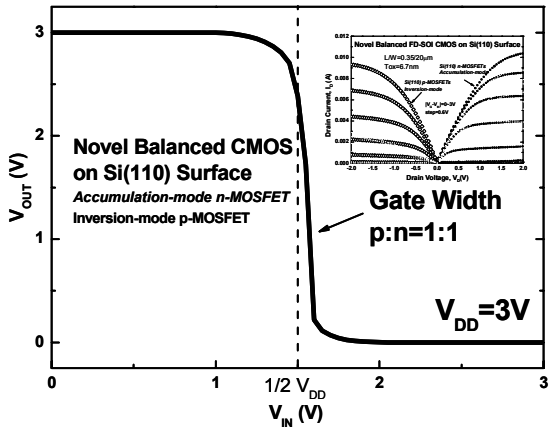

Fig. 6 The ideal V_{in}-V_{out} characteristics of the novel balanced CMOS inverter with AM n-MOSFET and IM p-MOSFET on Si(110) for gate width ratios of pMOSFET/nMOSFET=1:1.

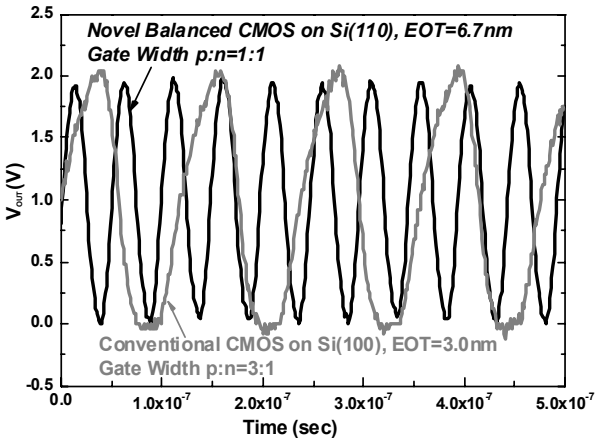

Fig. 7 The oscillation frequency of 101 stages of inverter chains for the same gate width in balanced CMOS on Si(110) is about 2 times higher than that of conventional CMOS fabricated on Si(100) surface.

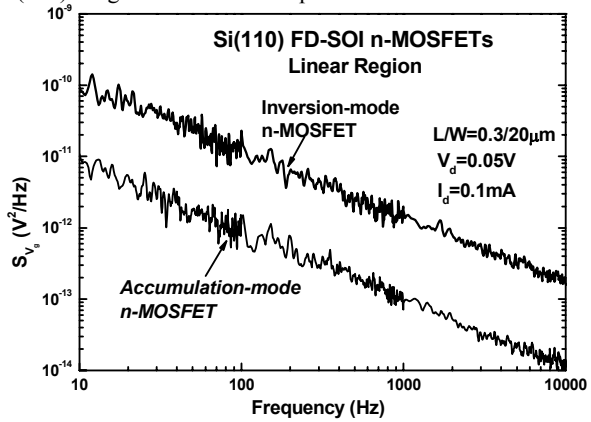

Fig. 8 1/f noise level in AM n-MOSFETs operated at linear region on Si(110) is suppressed about 1 digit compared with that in IM n-MOSFET.

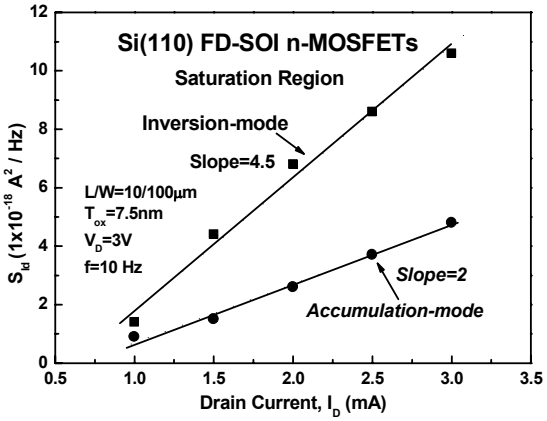

Fig. 9 1/f noise levels in n-MOSFETs on Si(110) operated on saturation region as a function of drain current. The slope for AM n-MOSFETs is much smaller than that for IM n-MOSFETs.