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Comparison of plasma doping with implant for high performance SOI CMOS fabrication

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Abstract

New approaches have been developed to match plasma doping with ion implant for ultrashallow junction formation.This newly matched plasma doped extension junctions have been successfully implemented with other advanced device process elements such as SMT, e-SiGe and dual stress liners to ***achieve highest performance SOI CMOS devices yet reported with plasma doping*** ; PFETs and NFETs I_{on} at I_{off} of 100 nA/μm are ~ 800 and ~ 1000 μA/μm (V_{dd} = 1V) respectively. DIBL and subthreshold slope are ~ 200 mV amd 100 mV/decade. Junction diode and large area, thin gate dielectric capacitor leakages are comparable to corresponding high performance CMOS with I/I extension. High performance RO with I/I NFETs and plasma doped PFETs achieving a stage delay of 9.9 ps (IDDQ=80 nA/st/µm) with a fanout of 3 have also been demonstrated.

1.Introduction

For continued scaling of future CMOS device, heavily-doped ultra-shallow extension junctions (< 30 nm Xj) are required. For these USJ requirements, plasma doping(PD) offers an attractive alternative to I/I for its capability of achieving high dose, low energy doping for shallow and abrupt USJ formation[1,2]. In addition, other aspects of PD parameters such as molecular source, diluent species[3] and plasma deposition temperature[4] can further be explored to improve USJ activation. In this work, focus will be on development of matching PD to high performance device I/I extension and integration of matched PD extension for high performance SOI device fabrication. The following sections compare SOI CMOS performance with PD and I/I extension in detail.

2. Matching Plasma doping with I/I

For device performance comparison, plasma doping (PD) and I/I will be used for the formation of USJ in the device extension region. The first step taken is matching PD with I/I profiles designed for high performance PFET and NFET devices. Fig.1 shows B I/I profiles with tilt and no tilt. As shown, shallower B junctions are achieved with tilt where B channeling is reduced. The other matching boron PD profiles labeled with BF_3 plasma condition 1, 2 & 3 shown in Fig.1 are generated with plasma potential bias close to I/I energy. As shown, most of the PD profiles resemble I/I with no tilt indicating that PD doping essentially has zero degree tilt. Matching of shallower B profile with tilt I/I can be achieved with a combination of changes in plasma bias potential, pressure and exposure times. These results are demonstrated in Fig.2. It is found experimentally that for given plasma potential bias and source pressure, the doses for the PD increases linearly with time. These results are shown in Fig.3 for B and As doping. This feature is particularly useful for device centering where a matrix of well defined extension doses are used for performance optimization. As shown in Fig.4, successful matching of As I/I with AsH_3 PD has also been achieved with similar approaches.

3. Device fabrication

For assessment of the potential of PD for future technology device, the CMOS device fabrication with PD extension junctions was carried out in a high performance SOI device process route. SMT, e-SiGe S/D and dual stress liner are used in the process route for achieving high performance NFETs and PFETs. The PD for device extension junctions was carried out simply as a substitution for the extension I/I step. Device junction optimization was evaluated with high temperature spike RTA anneal or a combination of high temperature spike RTA + milli-second laser anneal. Device centering and optimization were carried out with a matrix of spacer, extension and halo conditions. On wafer SIMs and Rs analysis were used to assess the PD and I/I device extension junctions which went through the entire device thermal budget process sequence through metallization.

4. Device results and Discussion

4.1 Device junction and leakage comparison

Fig.5 shows a comparison of on-wafer PFETs boron extension junction profiles created with PD and I/I. The S/D anneal for the junction is a high temperature spike RTA only. As shown, comparable B junction depth and abruptness are achieved except for the differences in the B concentration near the plateau region. Additional analysis of integrated atomic dose and junction Rs indicate that B activation in PD junction is better than I/I(> 20%). Fig.6 shows a comparison of on wafer NFETs As junctions created with PD and I/I. The S/D anneal for both was high temperature spike RTA only. Apparently due to increase in actual PD dose than estimated , there is a corresponding increase in As junction depth and concentration. However taken together the additional information on atomic doses and junction Rs suggest that As diffusion and activation in device PD and I/I junctions are quite comparable. Fig.7 shows comparison of measured junction diode characteristics for PFETs and NFETs with junctions created with PD and I/I. As shown comparable forward and reverse characteristics are achieved for both cases for PFETs and NFETs. These agree with results from a comparison of TEM x-section micrographs of PFETs with I/I and PD extension junctions shown in Fig.8 and Fig.9. As shown, no obvious defects are observed in extension and e-SiGe S/D regions for both cases. Similar TEM results were also observed in NFETs with PD and I/I junctions.

4.2 Device performance and gate leakage comparison

Fig.10 shows a comparison of measured I_d -V_{gs} characteristics of NFETs with PD and I/I extensions. As shown matching high performance NFETs are achieved in both case with I_d ~ 1000 μA/μm at Vdd =1V and sub-threshold slope of ~ 100 mV/decade. Fig.11 shows a comparison of corresponding measured I_d -V_{gs} characteristics of PFETs. This result also demonstrates matching high performance PFETs with PD and I/I extensions with I_d ~ 800 μA/μm at Vdd =1V and sub-threshold slope of ~100 mV/decade. Fig.12 shows that comparable I_{off} -I_{on} characteristics are achieved for PFETs and NFETs with PD and I/I extension at matched C_{ov}. The measured I_{on} at I_{off} of 100 nA/μm are ~ 700 μA/μm (PFETs, V_{dd} = 0.9 V) and ~ 1000 μA/μm (NFETs, V_{dd} = 1V) respectively. Similar DIBL (N & PFETs Fig.13, Fig.14) and Vt_{sat} roll-off characteristics (N & PFETs Fig.15, Fig.16) are also achieved which suggest similar SCE behavior of N & PFET devices with PD and I/I extension . Fig.(17) shows a comparison of gate leakage from large area multi-finger gate capacitors(~30 μmx30µm) for PFETs and NFETs. The fact that similar level of gate leakage are obtained over a large gate capacitor area demonstrates that damage to thin gate dielectric during plasma doping is minimal in these cases. Fig.18 show a comparison of output waveforms from RO with I/I P & NFETs and RO built with I/I NFETs and PFETs with PD junctions. As shown, matching high performance RO with stage delay of ~ 9.9 ps at IDDQ ~ 80 nA/st/µm with a fanout of 3 has been achieved in both cases.

5. Conclusion

High performance SOI CMOS with PD extension have been successfully demonstrated ; PFETs and NFETs I_{on} at I_{off} of 100 nA/μm are ~ 800 and ~ 1000 μA/μm (V_{dd} = 1V) had been achieved. Measured SCE, junction diode and large area thin gate dielectric capacitor leakage characteristics are comparable to the corresponding high performance CMOS with I/I extension . These results demonstrate the potential of PD as a low cost , high throughput alternative to low energy high dose I/I for future high performance SOI CMOS device fabrication.

6. Reference

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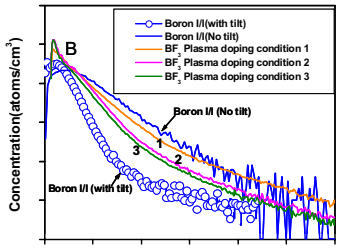

Fig.1 Comparison of I/I and plasma doping boron profiles

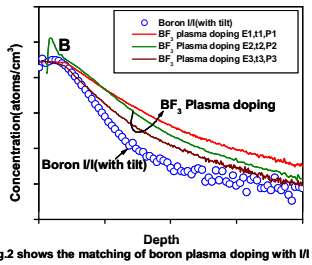

Fig.2 shows the matching of boron plasma doping with I/I with combinations of plasma doping bias(E), time(t) and pressure(p)

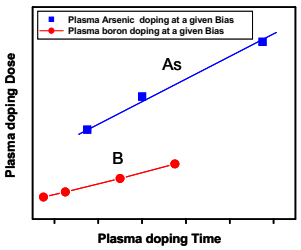

Fig.3 shows plasma doping dose increases linearly with plasma doping time(t)

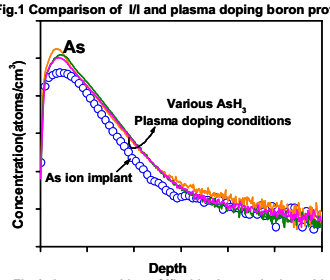

Fig.4 shows matching of I/I with plasma doping with combination of bias, pressure and doping time

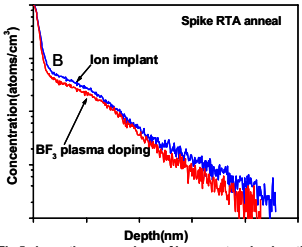

Fig.5 shows the comparison of boron extension junction profiles for I/I and Plasma doping after spike RTA

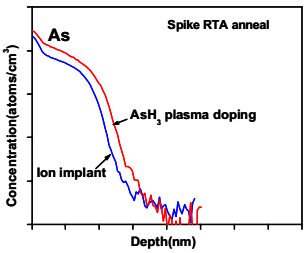

Fig.6 shows the comparison of arsenic extension junction profiles for I/I & Plasma doping after spike RTA

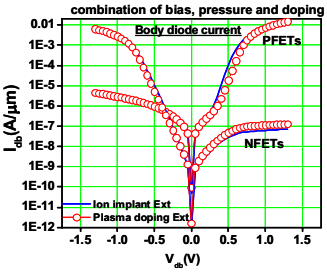

Fig.7 Comparson of I_{db}–V_{db} for P&NFETs diodes with I/I and P&NFETs diodes with plasma doping junctions

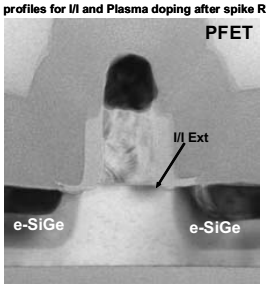

Fig.8 TEM X-section of PFET with I/I Ext & e-SiGe S/D. No Obvious defects in extension and e-SiGe S/D

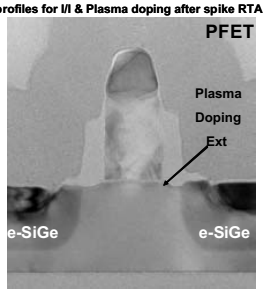

Fig.9 TEM X-section of PFET with plasma Ext, plasma & I/I e-SiGe S/D. No obvious defects in extension & e-SiGe S/D

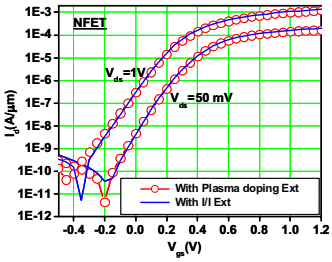

Fig.10 Comparison of I_d –V_{gs} for NFET with I/I and NFET with plasma doping extension junctions

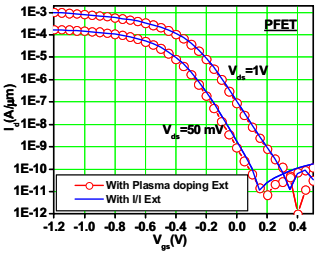

Fig.11 Comparison of I_d –V_{gs} for PFET with I/I and PFET with plasma doping extension junctions

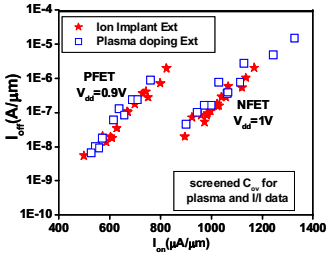

Fig.12 shows comparable I_{off} –I_{on} for P&NFET with I/I and P&NFET with plasma doping extension junctions

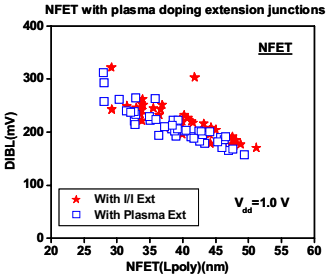

Fig.13 shows comparable DIBL-Lpoly for NFET with I/I and NFET with plasma doping extension junctions

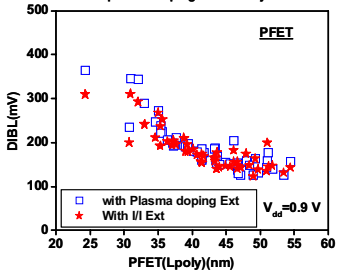

Fig.14 shows comparable DIBL-Lpoly for PFET with I/I and PFET with plasma doping extension junctions

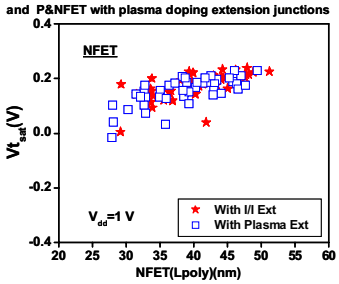

Fig.15 shows comparable Vt_{sat}-Lpoly for NFET with I/I and NFET with plasma doping extension junctions

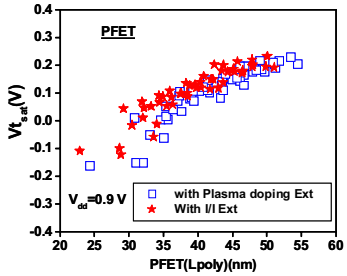

Fig.16 shows comparable Vt_{sat}-Lpoly for PFET with I/I and PFET with plasma doping extension junctions

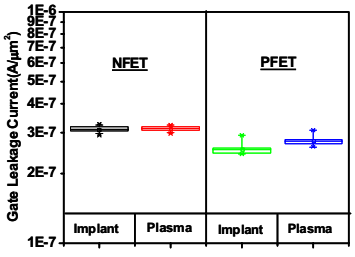

Fig.17 shows comparable gate leakage of multi-finger large area gate capacitor(30 umx30 um) for P&NFET with I/I & P&NFET with plasma doping

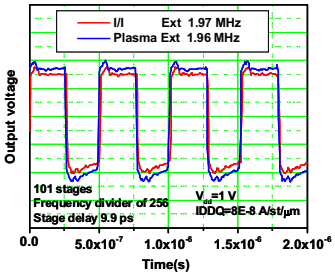

Fig.18 shows comparable RO characteristics for RO with I/I P&NFETand RO with I/I NFET and Plasma PFET