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Evaluation of Threshold-Voltage Variation in Silicon on Thin BOX (SOTB) CMOS and Its Impact on Decreasing Standby Leakage Current

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1. Introduction

Increasing power consumption is a serious problem in the current scaled CMOS because the supply voltage does not scale down proportionally and the standby leakage current increases. The major cause of this problem is widely recognized to be increasing threshold-voltage (V_{th}) variation.

We proposed a new FDSOI structure (Fig. 1) named Silicon on Thin BOX (SOTB) [1], which can be controlled by the back-gate bias, and have shown that it has a small V_{th} variation about half that of the conventional bulk CMOS [2]. In this study, we systematically investigated the V_{th} variation of SOTB and estimated the effect of a small V_{th} variation on decreasing the leakage current.

2. Electrical Characterization of Devices

SOTB devices were fabricated by a process based on the 65-nm low-power CMOS flow combined with additional raised source/drain and fully silicided (FUSI) gate processes. Details were described elsewhere [2, 3].

V_{th} values were determined from I_d-V_{gs} characteristics at various gate lengths (L_g) and widths (W_g) within a wafer. We used the saturation extrapolation method at V_{ds} = 1.2 V in most cases. A typical cumulative probability plot of V_{th} values is shown in Fig. 2. Note that σV_{th} for PMOS is always smaller than that for NMOS, that is, the slope of the plot is steeper with the same gate size and $|V_{th}|$, as pointed out for the conventional bulk CMOS in [4]. The number of sampling points was restricted to less than 40 in a wafer, and thus we performed the D'Agostino-Pearson test [5] to confirm the normality of distribution. Results are shown in Table I. We can conclude that the distribution could be normal because K^2 values are less than the critical value of 5.99.

Pelgrom plots for the NMOS of different gate materials and halo implant are shown in Fig. 3. The slope of the plot, namely, the Pelgrom coefficient A_{Vt}, is an indicator of V_{th} variation. The A_{Vt} values are summarized in Table II. The values for bulk devices are shown based on the result in [4] assuming the same capacitance equivalent oxide thickness ($T_{ox\text{-}inv}$) and V_{th}. The A_{Vt} value for SOTB with halo implant and poly-Si gate was higher than that of the bulk, although the same process as the bulk was used. This might be because the halo implant significantly increased the statistical variation of impurity due to the confinement of the halo implant within a thin SOI layer (10-15 nm). Thus, we concluded that the halo implantation is harmful to the variability in SOTB. Unlike the bulk, SOTB can effectively suppress the short-channel effect without the halo implantation because of both ultrathin SOI and BOX layers [2]. This leads to a significant decrease in A_{Vt}. By using the FUSI metal gate, the value further decreased to half that of the bulk. Decreasing $T_{ox\text{-}inv}$ by 0.4 nm due to suppressing gate depletion and the absence of the poly-grain effect might contribute to decreasing A_{Vt}. $\sigma(V_{th}^F - V_{th}^R)$ values are shown in Fig. 4 for the same samples as in Fig. 3. These values, obtained by exchanging source and drain [6], are indices of local (mainly statistical) variation. The result strongly suggests there is a significant decrease in local variation in

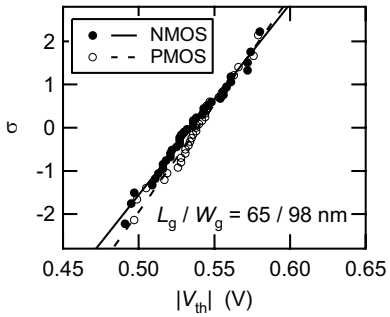

Fig. 2 Cumulative probability plot of V_{th} for N and PMOS.

Table I Results of D'Agostino-Pearson test

	NMOS	PMOS
average V_{th} (V)	0.535	-0.539
σV_{th} (mV)	22.4	20.0
K^2	0.859	0.384

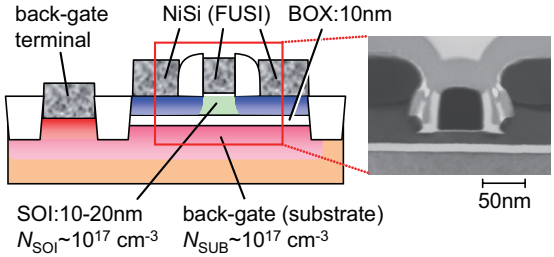

Fig. 1 Schematic cross-section of SOTB transistor. Features: (i) Small σV_{th} due to low N_{SOI}, (ii) Excellent short-channel-effect immunity due to thin SOI and BOX, (iii) Back-gate bias control capable of trimming V_{th} and performance boosting. (iv) I/O bulk transistors can be integrated.

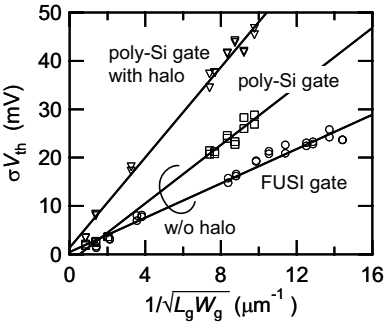

Fig. 3 Pelgrom plot (σV_{th}) for NMOS of several gate materials and halo implant.

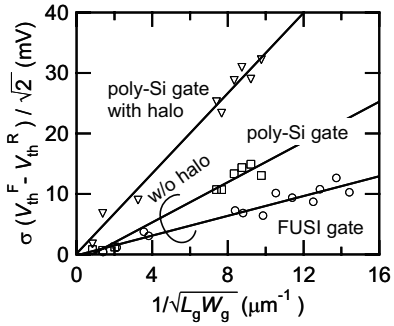

Fig. 4 Pelgrom plot ($\sigma(V_{th}^F$-$V_{th}^R)/\sqrt{2}$: indicator of local variation) for same samples as in Fig. 3.

Table II A_{Vt} values for various structures

structure	gate	halo	A_{Vt} (N)	A_{Vt} (P)
SOTB	Poly-Si	yes	4.8	4.5
SOTB	Poly-Si	no	2.8	3.6^{+}, 2.5$^{\#}$
SOTB	FUSI	no	1.8	1.5
Bulk*	Poly-Si	yes	3.6	2.2

* Assuming $T_{ox\text{-}inv}$=2.7 nm and V_{th}=0.5 V
$^{+}$ Due to short-channel effect, $^{\#}$ Linear condition (V_{ds}=-0.05 V)

the FUSI SOTB.

Dependence of σV_{th} on drain voltage (V_{ds}) is shown in Fig. 5. The V_{th} values were determined by the constant current (10^{-9} A/μm) method. It is notable that the dependence of σV_{th} for the FUSI device was very weak because the short-channel effect was well suppressed. For the $\sigma(V_{th}^{F}$-$V_{th}^{R})$ values, there was a strong V_{ds} dependence especially for the halo device. This is because of strong channel-length modulation caused by V_{ds} at about $V_{gs} = V_{th}$, that is, reduced channel length increases statistical variation just like decreasing L_g. The above results strongly suggest that using low-dose channel and not using halo is essential to decrease local variation. The SOTB is thought to be one of the ideal structures in terms of small variability.

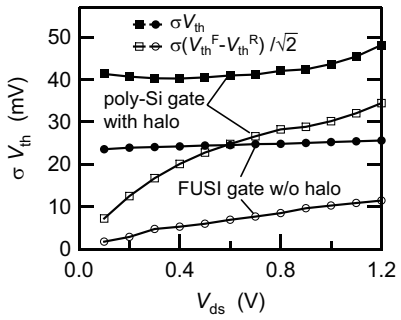

Fig. 5 Dependence of drain voltage (V_{ds}) on σV_{th} for SOTB NMOS. $\sigma(V_{th}^{F} - V_{th}^{R})/\sqrt{2}$ is shown.

3. Estimation of Leakage current

Increasing σV_{th} causes marked increase in leakage current of an LSI chip because it can contain a significant number of leaky transistors with an increasing number of transistors in a chip. Here we demonstrate a reduction in leakage current summing for a large number of transistors taking σV_{th} into account. The currents for the bulk and SOTB were compared. The conditions for the calculation are listed in Table III, assuming a SRAM chip fabricated by a 65-nm technology. I_{off} versus ΔV_{th} is shown in Fig. 6 (a). When decreasing V_{th} from the typical value, I_{off} increases due to subthreshold leakage. On the other hand, I_{off} also increases with increasing V_{th} because of gate-induced drain leakage (GIDL). A V_{th} probability plot is shown in Fig. 6 (b). σV_{th} of SOTB is half that of the bulk with the same device size. The expected value of I_{off}, $P \times I_{off}$, for each V_{th} is plotted in Fig. 6 (c). The integration of the hatched (painted) area corresponds to the summed leakage current. For one million transistors, these values are 54.7 and 28.2 μA for the bulk and SOTB, respectively. This result indicates that reducing σV_{th} by half has an impact of reducing leakage current by half for chips fabricated by the 65-nm technology. This effect continues to be enhanced with scaling (1/3 for 45 nm with half σV_{th}).

4. Conclusion

V_{th} variation of SOTB was studied. The low impurity concentration in the SOI layer without the halo implant is essential for maintaining small variability due to the reduced statistical variability component. The value of σV_{th} for SOTB is half that for the bulk. This corresponds to a reduction in the off-state leakage current of less than half.

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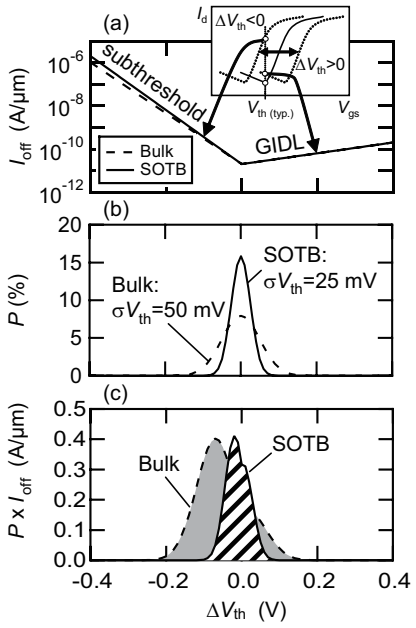

Fig. 6 Estimation of leakage current reduction by decreasing σV_{th}. (a) I_{off} versus ΔV_{th}, Inset indicates increase in I_{off} caused by change in V_{th} from the typical value. (b) Probability plot of V_{th}. (c) Expected value of I_{off}: $P \times I_{off}$.

Table III Conditions of leakage-current calculation

	Bulk	SOTB
A_{Vt} (mVμm)	3.6	1.8
L_g / W_g (nm)	55 / 90	55 / 90
σV_{th} (mV)	50.4	25.2
subthreshold slope (mV/dec.)	85	80
GIDL slope (mV/dec.)	400	400
typical V_{th} (V)	0.40	0.40
typical I_{off} (pA/μm)	20.0	20.0