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Effect of Poly/SiON gate stack combined with thin BOX and ground plane for low Vth and analog applications of FDSOI devices

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1. Introduction

The Fully-Depleted (FD) Silicon On Insulator (SOI) MOSFET is very promising for scaled CMOS technology generations. It provides an ideal subthreshold slope (~60mV/dec), reduced junction capacitances and a better control of short channel effects (SCE, DIBL). Recent papers [1,2] have demonstrated that the use of metal gate (MG) combined with high-k (HK) is very interesting for performance enhancement because it enables to naturally achieve a high threshold voltage (Vth) value compatible with low power applications while keeping the channel intrinsic. However a reduction of this threshold voltage is necessary for low Vth and for analog applications. Several approaches, for Vth modulation, have been proposed in literature such as work-function engineering or dual metal gate integration [3-5], but these different options are not easily manageable. For FDSOI devices one interesting way to modulate the threshold voltage is to use a thin BOX combined with ground-plane (GP) implantation [6]. In this paper we propose to combine a simple poly/SiON gate stack for FDSOI devices with low channel doping and thin BOX with GP implantation in order to achieve Vth (~0.2-0.3V) compatible with low Vth and analog applications. The viability of this structure is also examined through mobility, reliability, analog performances, variability and noise study and compared to FDSOI devices with high-k metal gate stack.

2. Choice of architecture and implantation conditions

For low power applications (LP) the Vth required is about (0.2-0.3V). Band-edge electrode (N+ polysilicon/SiON gate stack) as electrode on NMOS with thick BOX requires a high channel doping $\geq 4.10^{18}cm^{-3}$ (fig.1). As published in [6], the use of a GP with a doping of $5.10^{18}cm^{-3}$ under the BOX allows increasing the Vth by 100mV without adding doping into the channel. Thanks to the GP combined with a thin BOX the channel doping (Nch) can be relaxed down to $2.10^{18}cm^{-3}$ (for TBox 10nm) (fig.2). In addition, the use of a thin BOX combined with a GP enables to reduce DIBL. Using the MASTAR model [7] we have determined that the optimal BOX thickness should be around 20nm for Lg 32nm with Tsi 8nm to keep a DIBL<100mV (fig. 3). In order to dope the channel and the GP with one unique implantation boron for NMOS and Ph for PMOS have been used.

2. Process flow

The starting materials are 300 mm <100> UNIBOND^{TM} SOI wafers with BOX thicknesses of 20nm. SOI films were thinned down by thermal oxidation and wet etching to achieve a final thickness of around 8-10 nm. After MESA isolation, the channel/GP implantation is selectively done on NMOS and PMOS devices. A SiON dielectric of approximately 2nm is grown. A poly-Si layer of 70 nm is deposited for gate fabrication. A 193 nm lithography combined with trimming is performed to achieve the desired gate dimensions. The minimum gate length dimension measured on the wafers is around 25nm (fig.4). After an offset spacer of 10nm realization, a selective epitaxy of 10nm is performed in extension regions in order to reduce access resistance. Raised extensions are implanted. To finish Dshape spacers, S/D implantation (activated by a 1080°C RTP spikes anneal) and silicidation (NiPtSi) are realized.

3. Thin gate oxide experimental results

By varying the GP dose from $2.10^{13}cm^{-2}$ to $6.10^{13}cm^{-2}$ for NMOS and $6.10^{13}cm^{-2}$ to $1.4.10^{14}cm^{-2}$ for PMOS the long Vth varies from 0.2V (as expected) to 0.5V (figs.5 and 6). Both NMOS and PMOS Id(Vg) characteristics are presented on fig. 7 for channel doping of $6.10^{13}cm^{-2}$ (NMOS) and $1.4.10^{14}cm^{-2}$ (PMOS). Whatever the implant dose used, the Ion/Ioff is not degraded (figs.8 and 9) for NMOS and PMOS respectively). Only the impact of the long Vth shift is seen on short MOSFETs. By increasing the implant dose for NMOS and PMOS devices (figs.10 and 11), we observe strong low field mobility degradation as expected for higher channel doping. Despite this, the low channel doping variants ($2.10^{13}cm^{-2}$ (NMOS) and $6.10^{13}cm^{-2}$ (PMOS)) show peak mobility values similar to the ones of the undoped channel devices with high-k metal gate stack (degraded by stronger Coulomb scattering [9]). Regarding the NBTI (fig.12) of wafer with channel doping of $2.10^{13}cm^{-2}$, the values are better compared to the high-k/metal gate stack, certainly due to the absence of N species coming from the TiN metal gate and transferred into the pedestal oxide under the high-k, that considerably degrade NBTI [9]. The PBTI (not shown here is very good for the two types of gate material and whatever the channel doping).

4. Analog gain

In order to be used in a CMOS platform, FDSOI must be co-integrated with I/O devices. The EOT of analog device is around 2.9nm corresponding to a Vdd of 1.8V. Analog gain (g_m/g_d) measured for both I/O and core devices are plotted in figs.13 and 14. The gain values for the variants with $2.10^{13}cm^{-2}$ (NMOS) and $6.10^{13}cm^{-2}$ (PMOS) channel doping have been measured around 400 at Lg=1µm. The slightly lower value measured for the metal gate stack case with undoped channel is attributed to the presence of the high-k.

5. Matching

The matching (fig.15) of the channel doping variants ($2.10^{13}cm^{-2}$ (NMOS) and $6.10^{13}cm^{-2}$ (PMOS)) reveals that the values are similar to those of the typical LSTP bulk technology 4.7mV.µm [10]. However the value is slightly degraded as compared to the high-k/MG undoped channel [8] but is strongly degraded as the channel doping increases.

6. Noise

The curves fig.16 for NMOS and PMOS show a standard behaviour of the 1/f noise evolution with a plateau in the subthreshold range and a decrease proportional to I_{DS}^2 in strong inversion. A scaling effect could be noted for both NMOS and PMOS devices. This is a typical effect for devices with pocket implantations. Noise level of FDSOI with poly/SiON gate stack is in line with bulk devices however devices with high-k/metal gate stack are noisier by about 1 decade.

4. Conclusion

In this paper we demonstrate the possibility to use FDSOI devices with poly/SiON gate stack for low Vth and analog applications. Good mobility, analog performances, noise and reliability values have been demonstrated with the combination of a thin BOX and GP and light channel doping (dose around $2.10^{13}cm^{-2}$ (NMOS) and $6.10^{13}cm^{-2}$ (PMOS)). However the necessity of a strong channel doping to achieve high Vth values looks incompatible with LSTP applications because of the variability and mobility penalty. Then in case where low and high Vth are necessary a poly/SiON, high-k/metal gate co-integration can be envisaged.

Acknowledgements

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Reference:

[1] C. Fenouillet-Beranger et al, IEDM 2007, pp267-270; [2] A. Vandooren et al, SOI Conf 2005, pp221-222; [3] S. B. Samavedam et al, IEDM 2002, pp433-436 ; [4] S. Yamaguchi et al, VLSI 2006, pp192-193; [5] P.F. Hsu et al, VLSI 2006, pp14-15 ; [6] C. Gallon et al, SOI Conf 2006, pp17-18 ; [7] http://public.ITRS.net; [8] C. Fenouillet-Beranger et al, submitted ESSDERC 2008 ; [9] X. Garros et al, to be published in VLSI 08 ; [10] E. Josse et al, IEDM 2006, pp693-696

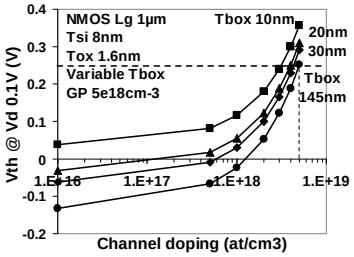

Figure 1: TCAD simulation of long NMOS linear Vth evolution versus channel doping for several BOX thickness with a GP doping of $5.10^{18}cm^{-3}$

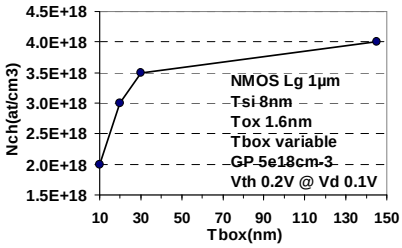

Figure 2: Channel dose necessary to obtain a long NMOS linear Vth around 0.2V versus BOX thickness with a GP doping of $5.10^{18}cm^{-3}$

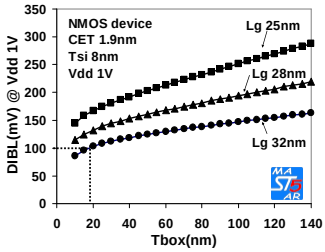

Figure 3: Optimal BOX thickness determination for NMOS FDSOI devices with Lg 32nm

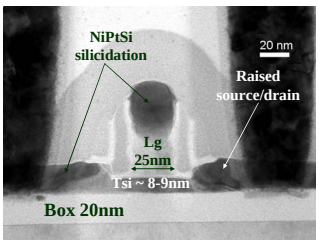

Figure 4: TEM cross-section of 25 nm nMOS FDSOI transistor with T_{BOX}= 20nm +GP

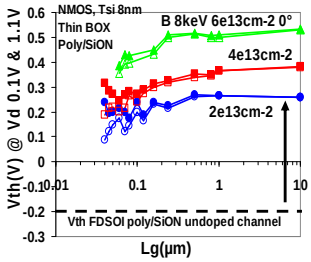

Figure 5: NMOS Vth(Lg) behaviour versus Nch/GP implant dose for FDSOI devices with BOX 20nm

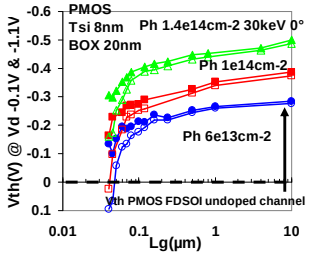

Figure 6: PMOS Vth(Lg) behaviour versus Nch/GP implant dose for FDSOI devices with BOX 20nm

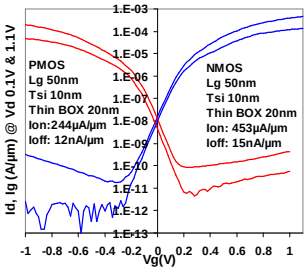

Figure 7: NMOS and PMOS Id(Vg) curves ($6.10^{13}cm^{-2}$ (NMOS) $1.4.10^{14}cm^{-2}$ (PMOS))

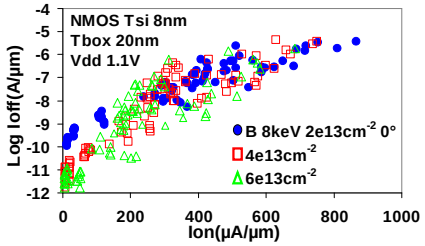

Figure 8: NMOS Ion/Ioff trade-off versus Nch/GP implant dose for FDSOI devices with BOX 20nm

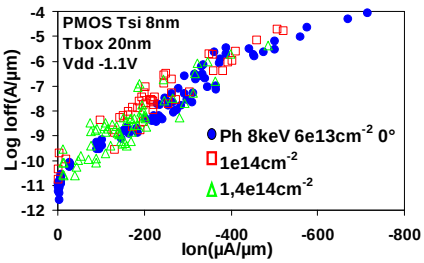

Figure 9: PMOS Ion/Ioff trade-off versus Nch/GP implant dose for FDSOI devices with BOX 20nm

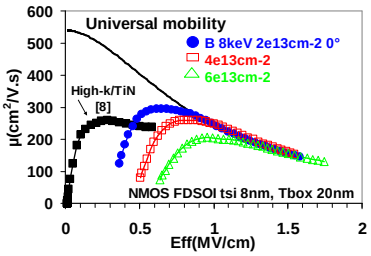

Figure 10: Mobility measurements from L=10µm NMOS devices with poly/SiON gate stack versus high-k/TiN gate stack

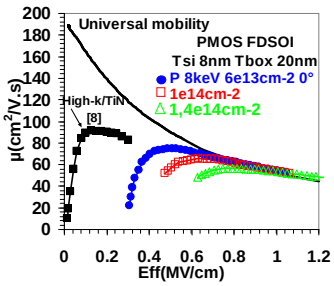

Figure 11: µ measurements from L=10µm PMOS devices with poly/SiON gate stack versus high-k/TiN gate stack

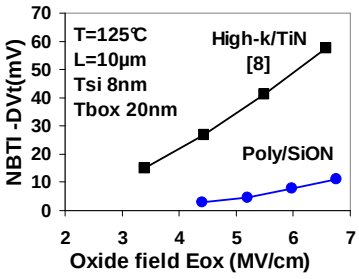

Figure 12: NBTI variation for FDSOI devices with poly/SiON gate stack ($2.10^{13}cm^{-2}$ NMOS) versus high-k metal gate stack @ Vd -0.1V

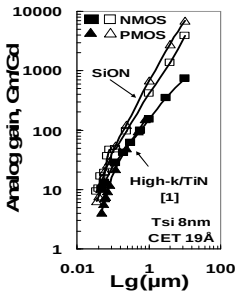

Figure 13: 19Å/dd 1.1V NMOS/PMOS core device analog performance.

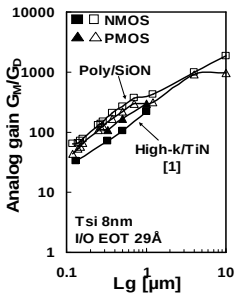

Figure 14: 29Å/Vdd 1.8V NMOS/PMOS IO analog performance. (Nch poly/SiON $6.10^{13}cm^{-2}$ PMOS)

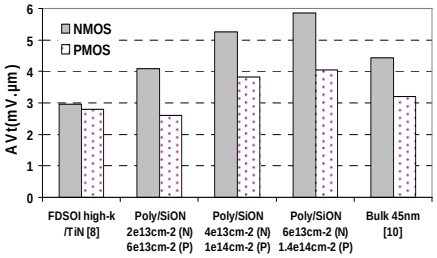

Figure 15: Linear Vth mismatch variation for NMOS and PMOS with various structure for area <0.1µm²

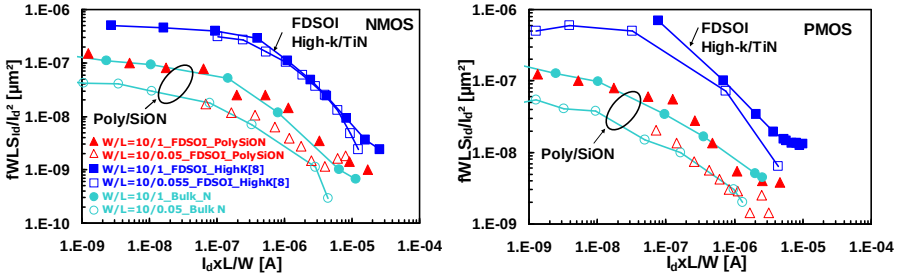

Figure 16: NMOS and PMOS variation of the normalized drain current 1/f noise level against Id*L/W at 1Hz for FDSOI devices (Poly/SiON ($2.10^{13}cm^{-2}$ NMOS; $6.10^{13}cm^{-2}$ PMOS)) or High-k/TiN gate stack) and bulk (Poly/SiON gate stack)