Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 48-49

C-1-1 (Invited)

Plastic Material Solutions for Advanced Thin Packages

Hiroyuki Tanaka
Sumitomo Bakelite Co. Ltd., Information and Telecommunication Material Laboratories
20-7, Kiyohara Industrial Park, Utsunomiya, Tochigi, 321-3231, Japan
Phone: +81-28-667-3259, E-mail: tanakah@sumibe.co.jp

1. Introduction

A flip-chip (FC) package with a lead-free solder bump is being introduced because of the demand for semiconductor packages with high frequency and multiple functions. On the other hand, thinner and lower-profiled packages are required in FC packages for hand-held products such as mobile telephones and digital cameras. Many plastic materials are applied as packaging materials in FC packages. In this study, thermo-mechanical characteristics of thin FC packages related to its reliability are analyzed against the physical properties of packaging materials using finite element method (FEM). Viscoelasticity of the underfill, which affects solder bump protection characteristics from external stress, is considered for detailed calculations in the analyses.

2. Thermo-mechanical characteristics of the FC package related to its reliability

Calculations of many kinds are necessary to clarify the thermo-mechanical reliability for FC packages in FEM analysis. The calculations were done for a FC ball grid array (FC-BGA) package in these analyses. Warpage at both room and reflow temperatures, solder bump fatigue during temperature cycling process, the energy release rate at the crack tip of low-*k* layer delamination, and stress in fillets of underfill were calculated against properties of packaging materials for the FC-BGA package. The structure of the FC-BGA package used in the analysis is portrayed in Fig. 1 along with the solder bump joint structure. Underfill is usually applied as an encapsulant for bump joints. Dimensions of the Si-chip are 15 mm × 15 mm × 725 μm. The package substrate comprises a substrate core with six build-up layers on it. The core thickness is 400 μm. The substrate size is 50 mm × 50 mm. The fillet length of the underfill is 1.7 mm. Software (Marc 2007 R1; MSC Software Co.) was used for FEM analyses. Temperature dependences of physical properties for all packaging materials were considered in FEM analyses, along with the viscoelastic properties for underfill and the elastic-plastic-creep properties for the solder bump.

3. UF properties

Temperature dependences of the modulus for the underfills (Underfill series A: A, AE1H, AE1L, AE2H, AE2L, Underfill series B: B, BE1H, BE1L, BE2H, BE2L) used in the FEM calculation are presented in Fig. 2(a) and Fig. 2(b). Temperature dependence of CTE for the underfills of series As and Bs are shown in Fig. 2(c). The T_g values are 45°C for series A and 75°C for series B.

4. Viscoelastic model used for calculations

Relaxation moduli and their temperature dependences for the underfills were determined from the temperature dependences of the dynamic modulus shown in Figs. 2(a) and 2(b) using a method described in a prior study [1]. As an example, a comparison of warpage values calculated using the elastic analysis to viscoelastic ones for a FC-BGA package is depicted in Fig. 3. The warpage values calculated using the two analysis methods differed greatly from each other at room temperature, confirming that the warpage values calculated using viscoelastic analysis agreed well with those for actual FC-BGA packages in the experiment.

5. Warpage analysis

Global warpage values calculated at 25°C for underfills are portrayed in Fig. 4(a). No elasticity dependence of warpage is shown, except for T_g dependence. A detailed analysis revealed that global warpage for FC packages was strongly affected by stress relaxation in the fillet of the underfill. Global warpage values calculated at a temperature of 260°C, which corresponds to the maximum temperature during the assembly process, are presented in Fig. 4(b). The global warpage values depend not only on the T_g value of the underfill, but also on the modulus. Warpage characteristics at 260°C are complex against the underfill properties.

6. Analysis of solder bump fatigue during temperature cycling

Figure 5 depicts the value of inelastic strain ranges of the solder bump in the FC-BGA package calculated in the condition of a temperature cycle of -55°C to 125°C, the cycle period was 1 h. The fatigue prevention levels of the solder bumps for the FC-BGA having underfills with larger T_g values are higher than those with a smaller T_g value. However, the higher fatigue prevention levels are explainable as the value of the modulus in the upper temperature ranges of T_g affecting the fatigue level of the solder bump; fatigue progresses in the temperature ranges of more than T_g during the temperature cycling test.

7. Si-chip damage analysis

Effects of underfill properties on delamination of low-*k* layers were also analyzed. Figure 6 shows the correlation coefficient between the energy release rate calculated at the tip of the delamination crack of a low-*k* layer, and the factor of underfill properties at -55°C. Results show that the delamination of low-*k* layers was affected strongly not only by the value of T_g of the underfill, but also by the CTE value. The Si-chip damage was also evaluated against the underfill properties using the calculation of the energy release rate at the tip of delamination crack of the underfill on the side wall of the Si-chip using FEM.

8. Influence of package substrate properties

Reliability of the FC package was also affected by the package substrate properties. Figure 7 portrays the warpage calculated for an FC-BGA having a thin conventional substrate with a 0.1-mm-thick core, which is compared to that with a core of 0.4 mm. The warpage of the FC-BGA package made of conventional substrate materials increases as the substrate thickness decreases. The warpage characteristics for a FC-BGA with a thin substrate having lower CTE and higher stiffness are shown in the figure. The warpage increases very little as the thickness of substrate decreases for substrates with lower CTE and higher stiffness. Figure 8 shows solder bump fatigue characteristics for the package with thin core with lower CTE and higher stiffness. The inelastic strain range does not increase as the substrate thickness decreases for the substrate with lower CTE and higher stiffness.

9. Conclusion

Effects of physical properties of packaging materials on the thermo-mechanical reliability of thin flip chip packages equipped with a lead-free solder bump were analyzed parametrically using FEM considering the viscoelasticity of underfills. Results show that a substrate with lower CTE and higher stiffness used for flip chip packages improved reliability without decreasing the T_g of the underfill.

Reference

[1] K. Miyake, "Thermo-viscoelastic analysis for warpage of ball grid array packages taking into consideration of chemical shrinkage of molding compound," JJIEP, Vol. 7, No. 1, pp. 54–61 (2004)

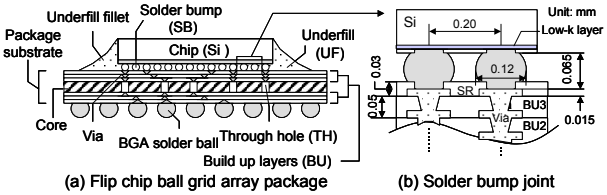

Fig. 1 Structures of the flip chip package and solder bump joint used in analyses

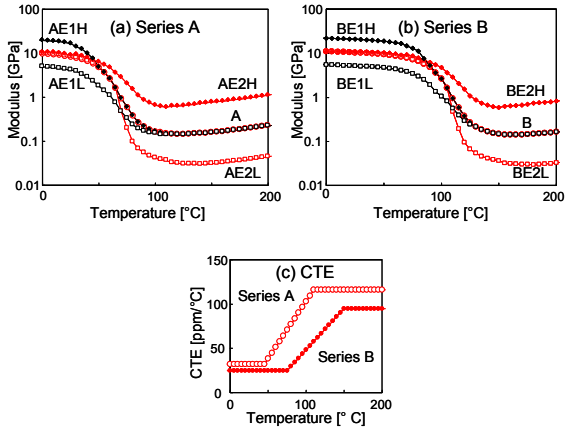

Fig. 2 Physical properties of underfills used in analyses: (a) Series A modulus, (b) Series B modulus, and (c) CTE

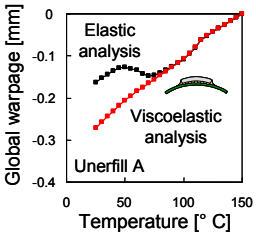

Fig. 3 Comparison of global warpage between analysis methods

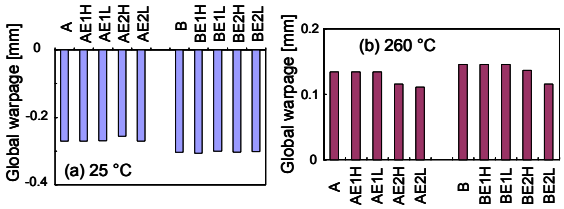

Fig. 4 Global warpage values calculated at (a) 25°C and (b) 260°C

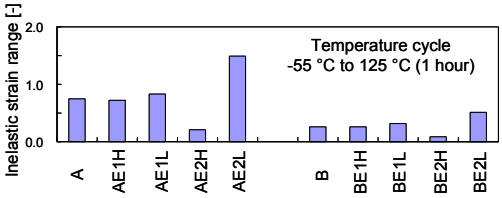

Fig. 5 Inelastic strain ranges of the solder bump in a temperature cycle of -55°C to 125°C

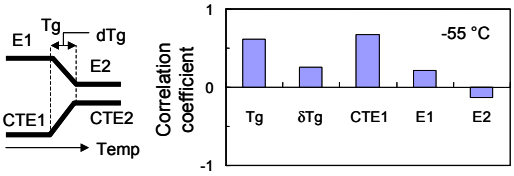

Fig. 6 Correlation coefficient between the energy release rate at the tip of the delamination crack of a low-*k* layer and the factor of underfill properties at -55°C.

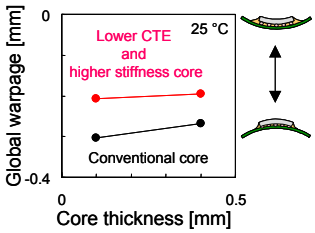

Fig. 7 Calculated warpage for FC-BGA packages with a thin substrate

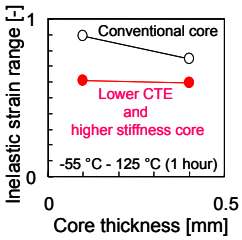

Fig. 8 Calculated inelastic strain ranges of a solder bump for FC-BGA packages with a thin substrate