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3D-Stacking Process for Si Interposer with integrated Thin-film Capacitors

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1. Introduction

Since the LSIs in digital electronic systems continue to operate faster, there is an urgent need to reduce the switching noise of the LSIs. Decoupling capacitors (DCCs) appear to be a promising countermeasure. A larger capacitance and smaller equivalent series inductance (ESL) for DCC are strongly required [1]. Using thin-film capacitors is effective, because they have a smaller ESL by their dielectric thickness in the nanometer range [2]. In order to minimize total parasitic inductance for LSI packages, mounting DCCs as close as possible to LSIs is important because the wiring between the LSI and the capacitor needs to be short. Therefore, a Si interposer integrated with thin-film capacitors has been developed. We used Mn-doped $SrTiO_3$ (STO) as a capacitor dielectric, because it has a paraelectric property at operating temperature, low leakage current and high reliability [3]. A cross-section of the stacked interposer is shown in Fig. 1. The capacitor has a large area corresponding with that of LSI. Because the interposer is directly connected and stacked with an LSI, it has an extremely low parasitic inductance. We report a technology suitable for fabricating large area thin-film capacitors on Si interposer and its novel stacking process that is based on a chip-to-wafer bonding technique.

2. Large Area Capacitor

Capacitors are fabricated by successively depositing a bottom electrode (BE), a 60 nm–thick STO, and top electrode (TE) films on thermally-oxidized Si wafer and patterning them with photolithography and etching to the Metal-Insulator-Metal (MIM) structure. Cavities are then formed on the wafer by deep reactive ion etching (RIE), and SiO_2 is deposited as an insulator and patterned. The cavities are then filled with Cu plating, which will become through silicon vias (TSVs). A top-view of the capacitor with cavities is shown in Fig. 2. The larger the capacitors are fabricated, the more short failures occur. In order to identify the leakage points of MIM, we performed an optical beam induced resistance change (OBIRCH) [4] analysis. Hillocks are observed in the MIM, in which STO was deposited at 600 ºC, as shown in Fig. 3. We found that the positions of hillocks are coincident with the leakage points. A cross-sectional SEM image of the interposer integrated with STO deposited at 400 ºC on Ru BE is shown in Fig. 4. While we observed no hillocks, we did observe sufficient Cu filling in the cavity. Consequently, a capacitance of 7 μF for a 20-mm □ interposer, which has 10,000 TSVs with a diameter of 50 μm, and a high capacitance density of 2.5 $\mu F/cm^2$ was obtained. The relationship of leakage current to voltage characteristics from -6 V to 6 V is shown in Fig. 5. No dielectric breakdown was observed in the range measured, and we achieved a low leakage current.

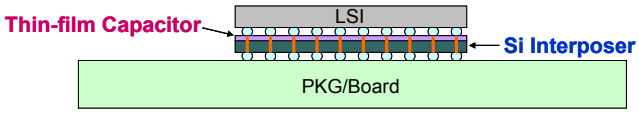

Fig. 1 Cross-sectional illustration of the stacked interposer.

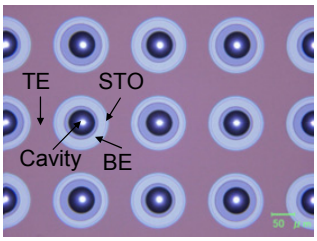

Fig. 2 Top-view of capacitor with cavities.

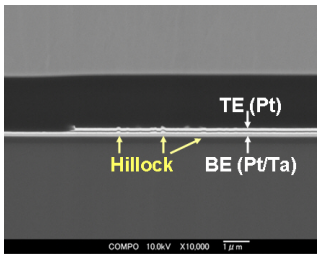

Fig. 3 Cross-sectional SEM image of hillocks at BE.

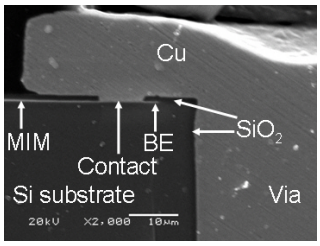

Fig. 4 Cross-sectional SEM image of the developed interposer.

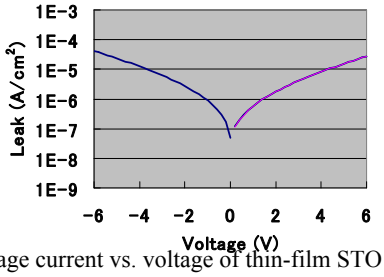

Fig. 5 Leakage current vs. voltage of thin-film STO capacitor.

3. 3D-Stacking

We used the chip-to-wafer bonding technique to carry out 3D-stacking for the interposer, and the process flow is shown in Fig. 6. First a wafer integrated with STO thin-film capacitors, cavities, which are filled with Cu conductors, and flip-chip bonding pads are directly connected to the conductors. Then, LSIs are bonded on the wafer by Pb-free solder bumps and under-filled with resin. After the Chip-to-Wafer bonding has finished, the wafer is molded with resin, and then thinned to a thickness of 50 μm through a vias opening. Photosensitive resin as an insulator and Cu pads are then formed on the backside of the wafer. Next, solder resist (SR) are coated and patterned. Finally, Pb-free solder bumps are formed and each stacked interposer with LSI is separated by cutting the wafer and resins. This process enables a 50 μm-thick interposer stacking with an LSI because the molding resin acts as a support while the wafer is thinned. The short via length of 50 μm reduces the LSI signals propagation delays. The stacked interposer with an LSI can be used as well as a bare LSI chip, and a 3D-stacked structure, i.e., one consisting of the LSI, the interposer, and the board, is obtained by bonding it to a board.

Cross-sectional SEM images of a test vehicle of interposer integrated with 1 μF capacitor are shown in Fig. 7. The 50 μm-thick interposer is stacked between the TEG chip and the PWB, and a short length of connection between capacitor and chip is achieved. The results of a thermal cycle (TC) test from -40 ºC to 125 ºC of 3D-stacked test vehicles is shown in Fig. 8. The 3D-stacked interposers exhibit a sufficient reliability of passing 1,000 cycles.

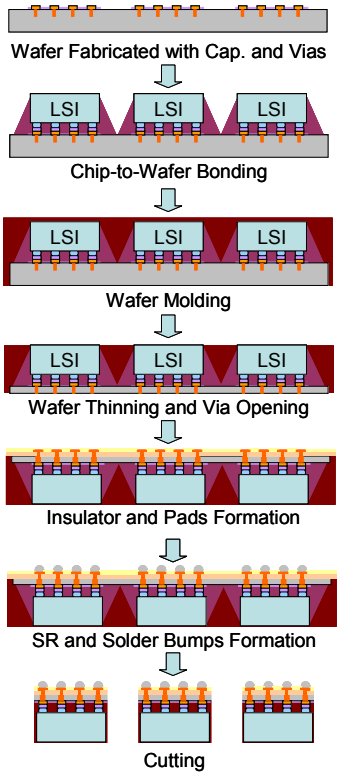

Fig. 6 Interposer stacking process flow.

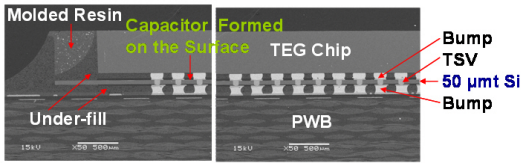

Fig. 7 Cross-sectional SEM images of 3D-stacked interposer.

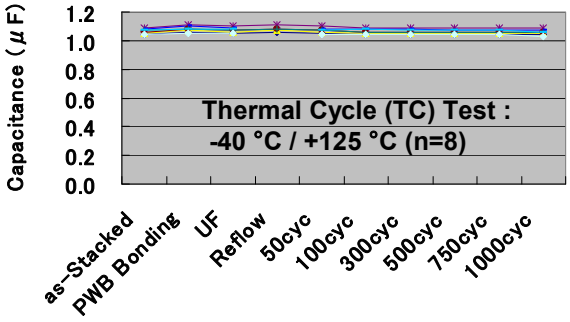

Fig. 8 TC result of 3D-stacked interposers.

4. Conclusions

We developed a Si interposer integrated with STO thin-film capacitors. Using the OBIRCH technique is a useful way to analyze the short failures for the large capacitors. A high capacitance density of 2.5 μF/cm^2 was obtained in a 20-mm □ area with 10,000 TSVs by depositing 60 nm-thick STO in MIM at 400 ºC. A novel 3D-stacking process based on Chip-to-Wafer bonding has also been developed. The developed process creates 50 μm-thick interposer stacking between an LSI and a board. The TC test of 3D-stacked test vehicles of interposer integrated with 1 μF capacitor exhibit a sufficiently high reliability of passing 1,000 cycles.

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