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A New Scaled Through Si Via with Polymer Fill for 3D Wafer Level Packaging

Deniz Sabuncuoglu Tezcan, Fabrice Duval, Ole Luhn, Philippe Soussan and Bart Swinnen

IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
Tel: +32 16 28 8741; Fax: +32 16 28 1576; Email: Deniz.SabuncuogluTezcan@imec.be

1. Introduction

Over the past 30 years and through scaling, the semiconductor industry has been able to continuously reduce the cost per function while simultaneously increasing the function density. More recently, 3D technologies emerged enabling further reductions in system form factors through stacking and interconnection of (partially) packaged devices. Today, many hand-held products contain stacked chips that are interconnected to each other via the package by means of peripheral wire bonds. The wire bonded 3D-interconnects are limited in terms of density and speed as they exhibit a high inductance. Through-Si vias (TSVs) provide an elegant answer to these limitations since they are naturally much shorter than wire bonds; and hence have better electrical performance.

Based on the type of manufacturing platform, IMEC is developing two types of TSVs for different 3D integration schemes [1]. When starting to process 3D interconnects on finished device wafers (CMOS or other), wafer level packaging (WLP) technologies are used. Fig. 1 shows IMECs concept for 3D-WLP technology where thin dies are stacked in a wedding-cake style by means of (micro-)bumps and TSVs.

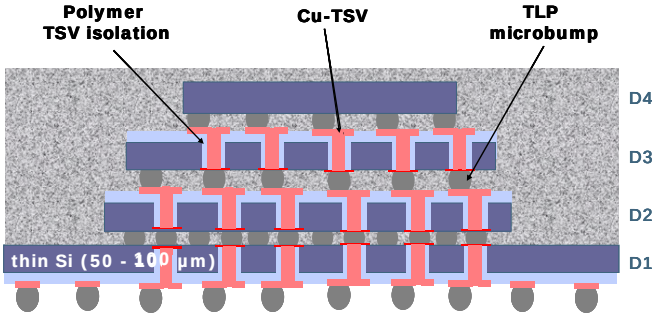


Fig. 1. Schematic view of IMECs 3D-WLP concept.

This paper describes the fabrication of a TSV technology for 3D-WLP integration; and it is designed for silicon substrates where interconnects are fabricated after standard CMOS processing and can be applied to any silicon based technology. Our previous approach, the sloped TSV process with CVD deposited parylene as polymer dielectric and conformal Cu plating was limited in scalability due to process limitations where the smallest via diameter was 50µm at the bottom and 100µm at the top for a wafer thickness of 100µm [2]. The new scalable TSV process described in this paper uses spin on polymer and bottom-up Cu via fill. Fig. 2 shows the schematic cross-section of this scaled via with target dimensions of 40µm pitch and 25µm via diameter for a wafer thickness of 50µm.

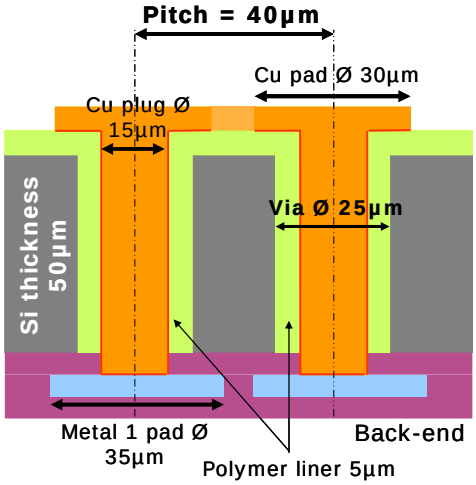


Fig 2. Schematic cross-section of the scaled via with target/designed dimensions.

2. TSV Fabrication

Figure 3 shows the schematic process flow of the scaled via. It is a thinning-first approach where the wafer is first bonded face down on a glass carrier using temporary glue and subsequently thinned to 50µm (Fig. 3(a)). Pyrex glass is used as the transparent carrier as it is CTE matched to Si. Then the first litho process is performed at the back of the wafers using front to back alignment through the transparent carrier to define ring patterns. Ring trenches of the TSVs are etched in thinned Si by standard Bosch RIE-ICP, i.e., deep reactive ion etching (DRIE), using resist as mask (Fig. 3(b)). DRIE process is independent of the FEOL and BEOL layer configuration of the device wafer; and the PMD layer serves as an etch stop.

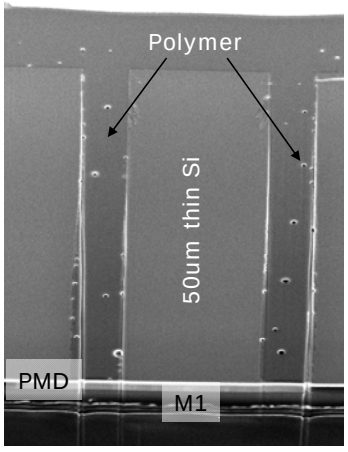
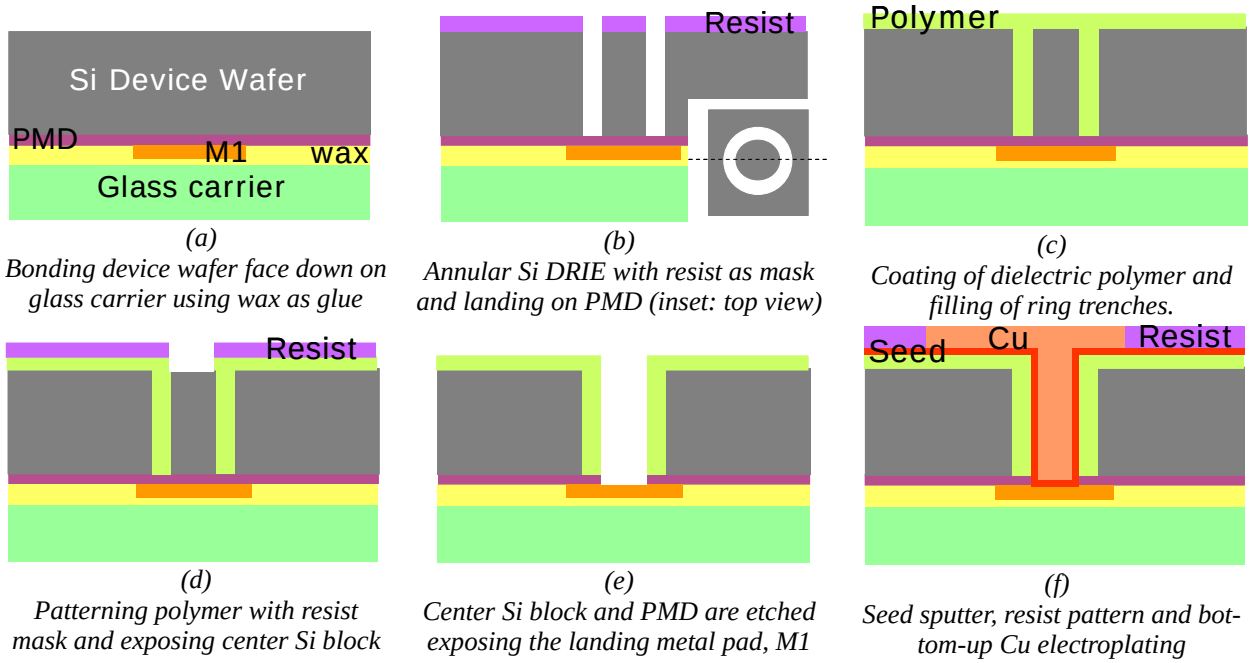


Fig 4. FIB cross-section of after polymer fill (Figure 3(c)).

Next are the stripping of the resist and the coating of dielectric polymer that will serve as the via insulation material. The main challenge of this process is the filling of the ring trenches with the polymer. A Special process is developed for this purpose using spray coating technique on a heated chuck and direct cure of the polymer [3] (Fig. 3(c) and Fig. 4).



(a) *Bonding device wafer face down on glass carrier using wax as glue*

(b) *Annular Si DRIE with resist as mask and landing on PMD (inset: top view)*

(c) *Coating of dielectric polymer and filling of ring trenches.*

(d) *Patterning polymer with resist mask and exposing center Si block*

(e) *Center Si block and PMD are etched exposing the landing metal pad, M1*

(f) *Seed sputter, resist pattern and bottom-up Cu electroplating*

Fig 3. Schematic process flow of scaled via.

Use of thick (5µm) polymer is a differentiator from most classical approaches in which via isolation is realized using CVD oxide or nitride layers with typical thicknesses between 50-150nm. For the given TSV diameter and depth, this results, however, in a high electrical capacitance value for the TSV, exceeding the capacitance of standard wire-bond pads. Using a thick polymer significantly reduces the capacitance and hence improves the electrical performance. A further advantage of using a thick polymer is that it can absorb some of the stress induced by the CTE mismatch between the Cu in the via and the surrounding Si. After polymer fill, the second litho is made to patterned the polymer on top of the center Si block. The polymer is etched by RIE using resist as mask (Fig. 3(d) and Fig. 5).

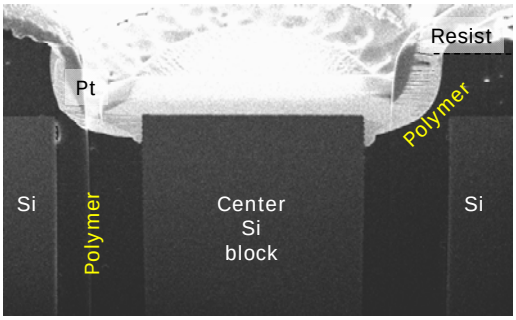


Fig 5. FIB cross-section of scaled via top after polymer pattern (Figure 3(d)).

Next the center Si block is etched by DRIE and the etching is again stopped on the PMD layer. The PMD layer is wet etched using a diluted HF solution with limited undercut (<1µm) exposing the landing metal pad which is fore seen on the device wafer front (Fig. 3(e)). Then the resist is stripped and the titanium/copper seed layer is deposited. The third and the last litho of the via process is made for the consecutive electroplating of Cu layer which serves as the main conductive path between the silicon wafer front and back. Using a plating bath with model additives [4], we demonstrated a bottom-up TSV fill with and simultaneous plating of 5µm routing lines on the field of the wafer (Fig.3 (f) and Fig. 6).

Finally, the plating resist and the seed layer are removed. Optionally another layer of the dielectric polymer can be spin coated passivating the Cu lines and prepare the wafer for bump process. All processes employed in the fabrication of the scaled via are performed at low temperature (<190°C) for post CMOS compatibility.

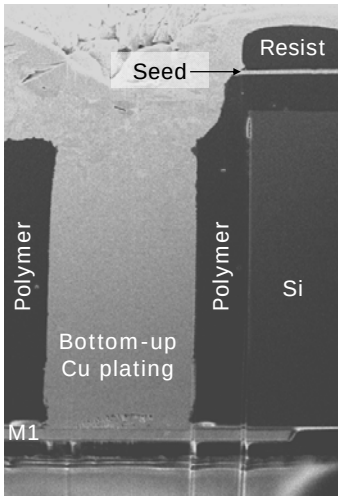


Fig 6. FIB cross-section of Cu plating (Figure 3(f)).

3. Conclusions

A new scaled and generic through wafer via process is developed using spin on dielectric polymer as isolation layer where ring trenches in Si are filled with this polymer. It is a via-last TSV process which is applicable to any silicon technology.

Acknowledgements

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References

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[4] O. Luhn et al., *Electrochemical Transactions* 6 (8) (2007) 123.